INSTITUT NATIONAL DES SCIENCES APPLIQUEES DE TOULOUSE

Getting started manual of Cadence v 6.1

Summary of the design kit AMS Hit-Kit H35 v4.10

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This manual aims at helping you to get familiar with Cadence and especially the schematic capture and simulation environment Virtuoso Design Environment v6.1 ®. The design kit AMS Hit Kit H35 v4.10 ® is used as example through this manual, which provides a rapid summary of the feature of this design kit. More information about Cadence and AMS design kit are available on-line at AIME.

Contents

I. Presentation of Cadence software

Cadence is a design environment which offers a complete design suite with a set of tools dedicated to:

- integrated circuit (IC) design
- high level simulation
- full custom IC layout.

This environment proposes about 480 tools. Figure 1 describes the typical design flow of an analog CMOS circuit in Cadence, from the schematic diagram capture to its validation (the layout and tape-out stage is not shown in this figure). An integrated circuit is an assembly of several subblocks. Each block is designed and validated individually before the assembly. In Cadence, a schematic diagram models one subblock.

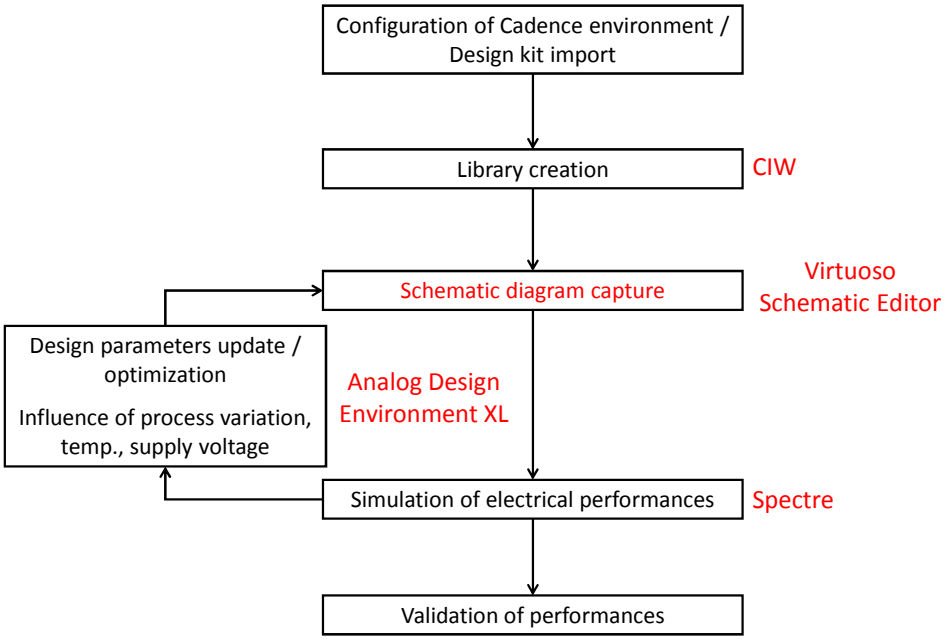

Figure 1 – Design flow of the electrical schematic diagram of an analog CMOS IC in Cadence

The launching of the environment must follow a configuration stage of environment variables. The design kit (see part II) is loaded during the launching in order to relate the electrical schematic to a technological process. The different schematics which model the subblocks of an IC must be organized in a library associated with a design kit. Cadence environment provides numerous tools accessible through a unique interface, such as schematic diagram saisie tool (e.g. Virtuoso Schematic Editor) and electrical simulation (e.g. Spectre). This course is limited to the optimization and the validation of electrical schematic diagram of analog CMOS circuits. This manual is only dedicated to the presentation of Virtuoso Design Environment.

II. Presentation of the design kit

The use of a design kit is required during all the design flow of an IC. The design kit includes the information related to a technological fabrication process in order to simulate the performances and design of ICs. It contains the electrical models of elementary components that can be made with the technological process (for example, CMOS devices, bipolar junction transistors, resistors, capacitors, I/O buffer, etc).

In this course, the design kit AMS H35 HIT Kit v4.10 from the foundry Austria Mikro Systems (AMS) is used. It includes design libraries related to the fabrication process High Voltage (HV) CMOS 50 V 0.35 µm, and a set of scripts to configure the Cadence environment automatically. In this course, the libraries linked to the process HV CMOS AMS 0.35 µm with 4 metal levels H35B4S1 is considered. Detailed information about this process are available in the document **ENG 238 - 0.35 µm 50 V CMOS Process Parameters**. This design kit contains the following libraries:

Library names	Library contents
CORELIB	Digital Standard Cells, 1.8 V – 3.3 V
CORELIB_3B	3-Bus Digital Standard Cells
IOLIBC_3B_4M	3-Bus Digital I/O Bidirectional Buffers and Power Pads
IOLIBC_4M	Digital I/O Bidirectional Buffers and Power Pads
IOLIBV5_4M	Digital I/O Bidirectional Buffers and Power Pads, 5 V supply
A_CELLS	Analog Standard Cells (Symbols and Layout Frames)
PRIMLIB	Primitive devices (NMOSFET, PMOSFET, BJT, resistors, capacitors)
PACKAGES	Package models (wire inductance and resistances)

Table 1- Libraries in the design kit AMS H35 HIT Kit v4.10

The library **analogLib** does not belong to this design kit but it includes a set of sources, symbols of voltage/current sources, passive and active devices.
The library **PRIMLIB** includes all the component fabricated with AMS design kit: MOSFET, BJT, diode, resistor, capacitor, inductor. In this course, MOS transistor models are:

- modn : model of NMOS low voltage 3.3 V
- modp : model of PMOS low voltage 3.3 V
- modni : model of NMOS low voltage 3.3 V isolated
- modpi : model of PMOS low voltage 3.3 V isolated
- modn20h : model of NMOS high voltage 20 V
- modp20h : model of PMOS high voltage 20 V

In this design kit, MOS transistor models are included in the file cmos53.scs (it can be read with any text editor) and provided for different process conditions (typical and worst case conditions). This file can be found in the directory: /soft/ams410/spectre/h35 (Figure 2). Transistor models are based on BSIM3 V3.

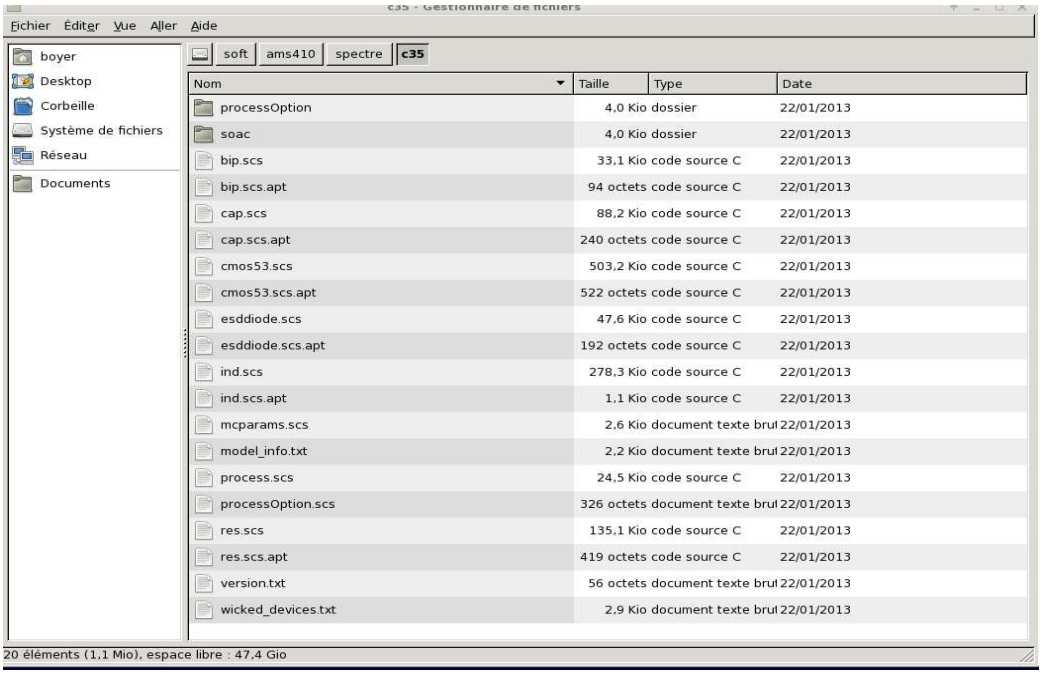

Figure 2 – Directory of the model files of the library PrimLib

```
//-------------------------------------------------------
// SPECTRE DIRECT
// MOS transistor library file
//-------------------------------------------------------
library cmos
section cmostm
//
// ---------------------------------------------------------------------
// Owner: Austria Mikro Systeme
// HIT-Kit: Digital
// ********************** SIMULATION PARAMETERS ***********************
//  ---------------------------------------------------------------------
//  format    : Spectre (Spectre Direct)
//  model     : MOS BSIM3v3
//  process   : C35
//  revision  : 4.0;
//  extracted : B10866 ; 2002-12; ese(5487)
//  doc#      : ENG-238 REV_4
//  ---------------------------------------------------------------------
//                          TYPICAL MEAN CONDITION
//
//  ---------------------------------------------------------------------
//
inline subckt modn ( d g s b )
parameters w=1.0e-6 l=1.0e-6 nrd=0.0 nrs=0.0 ad=0.0 as=0.0 pd=0.0 ps=0.0 ng=1
//
modn ( d g s b ) mosinsub w=w l=l nrd=nrd nrs=nrs ad=ad as=as pd=pd ps=ps m=ng
model mosinsub bsim3v3 version=3.2400e+00  type=n  capmod=2.0000e+00 \
 mobmod=1.0000e+00  nqsmod=0.0000e+00  noimod=3 \
     k1=5.0296e-01 \
     k2=3.3985e-02      k3=-1.136e+00      k3b=-4.399e-01 \
    nch=2.6110e+17 vth0=4.9790e-01 \
   voff=-8.925e-02    dvt0=5.0000e+01    dvt1=1.0390e+00 \
   dvt2=-8.375e-03    keta=2.0320e-02 \
 pscbe1=1.0000e+30  pscbe2=1.0000e-06 \
 alpha0=2.6000e-06  alpha1=5.0000e+00   beta0=2.1000e+01 \
  dvt0w=1.0890e-01   dvt1w=6.6710e+04   dvt2w=-1.352e-02 \
     ua=4.7050e-12      ub=2.1370e-18      uc=1.0000e-20 \
u0=4.7580e+02 \
   dsub=5.0000e-01    eta0=1.4150e-02    etab=-1.221e-01 \
```

Figure 3 – File cmos53.scs – Models of MOSFET

III. Create a working environment

Before launching Cadence, it is necessary to load the design kit in the working directory (where the design files will be saved). A new working directory is created from the console with the command **mkdir mon_repertoire**. Then, move into this new directory with the command **cd mon_repertoire**. Cadence environment can be launched from this working directory:

1. launch Cadence and load the design kit with the command **ams410**. Numerous environment variables are set during this stage.
2. specify to Cadence the used technological process in the design kit AMS H35 HIT-Kit. Type the command **ams_cds –tech h35b4 &**. A script is executed to load the technology CMOS 0.35 µm with four metal levels.

The environment is launching and the main window called **Command Interpreter Window** (CIW) appears (Figure 4). Cadence tools can be launched from CIW. All the messages appear on this window. After closing Cadence, it will be possible to relaunch Cadence environment by typing the command icfb & (icfb = Integrated Circuit Front-end to Back-end) from the working directory, since the design kit has laready been installed on this directory.

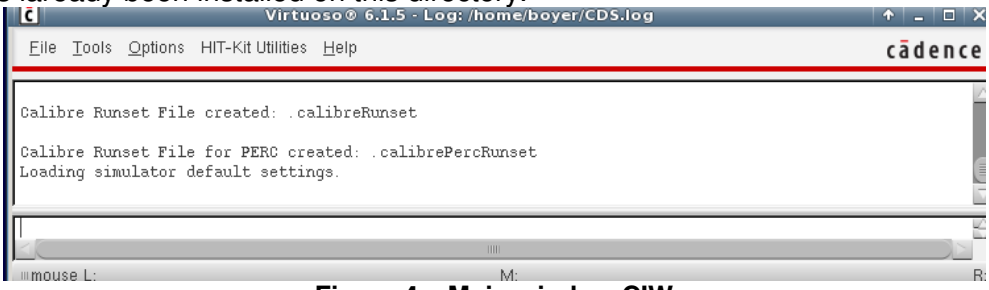

Figure 4 – Main window CIW

IV. Create a library

The next step is the creation of the working library, where the electrical schematic diagrams will be saved. From CIW, click on **File**/**New**/**Library**. The window shown in Figure 5 opens. Enter the name of your library in the field "Name" and select « Attach to an existing technology library » to attach a technological process to the library. A new window appears and select « Tech H35B4 ».

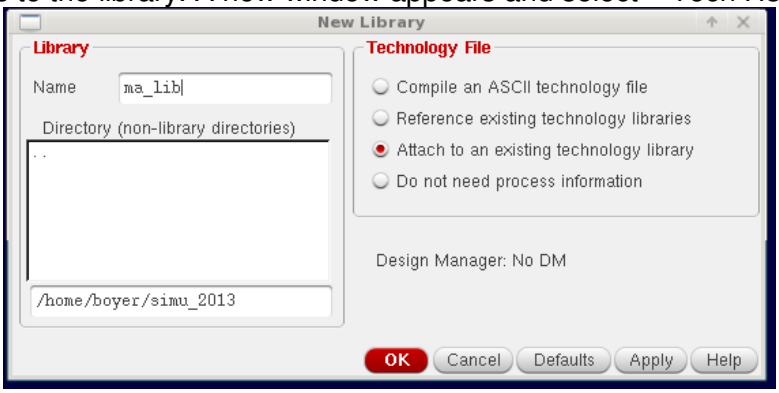

Figure 5 – Create a new library

The new library is visible in **Library Manager**. This window is extremely important for the navigation between the different libraries of components. You have access to it by clicking on **Tools**/**Library Manager** … The window shown below opens. It is formed by three or four categories:

- Library: it lists all the libraries of components
- Category: it can be hidden by checking Show Categories. The components of a library can be classified by categories (e.g. sources, active devices, passives, …)
- Cell: it lists all the components in a library
- View: it lists the different views of a given component (schematic diagram, symbol, layout, Verilog netlist…)

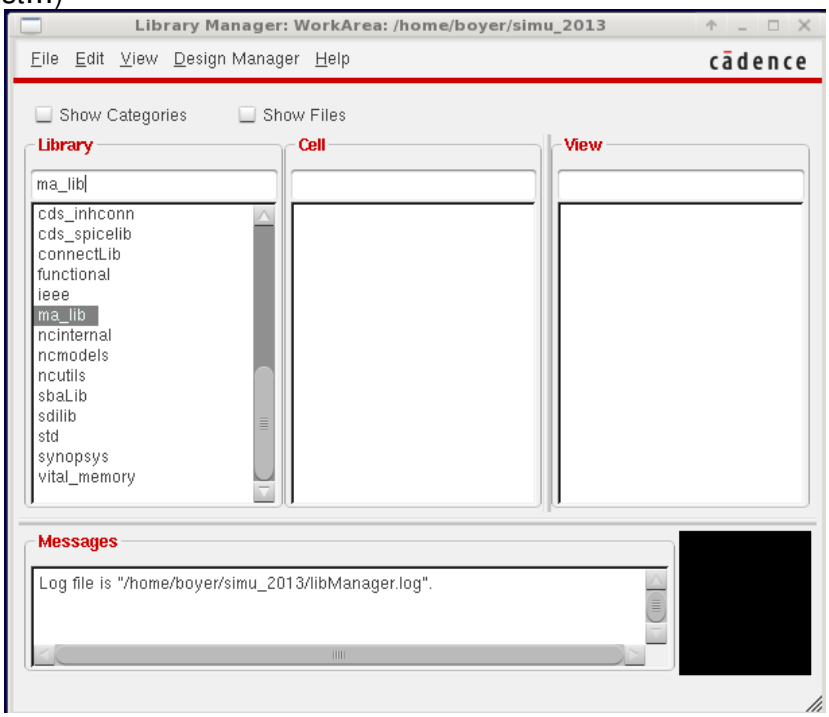

Figure 6 – Library Manager

If some libraries are lacking, they can be added by clicking on **Tools**/**Library Path Editor**, accessible from the CIW window. The name and the access path of the libraries will be specified. A cell and a view may also be opened from **Library Manager**.

V. Create a new cellview

The next step is the creation of a new cellview, which will include the schematic diagram view of the circuit that we want to design. Click on **File/New/Cellview**. The following window opens. Specify the name of the library, give the name of the new cellview and view that you are going to create. Select Schematic for the the type of view. The tool **Schematic_XL** will be used to construct the schematic diagram.

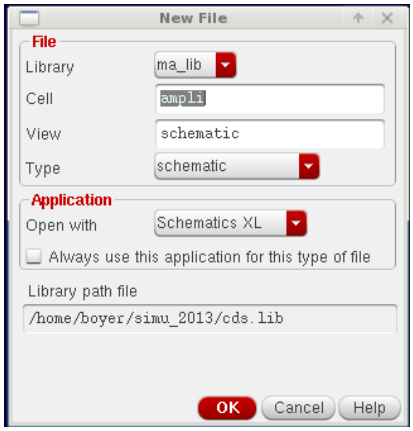

Figure 7 – Creation of a new cellview

Click on OK. The environment **Virtuoso Analog Design Environment XL** is loaded and the window **Virtuoso Schematic Editor XL** opens. The schematic diagram edition screen is blank. We can start the schematic diagram capture from scratch.

VI. Create an electrical schematic diagram with Virtuoso Schematic Editor

In order to illustrate the construction of a schematic diagram with Virtuoso Schematic diagram, let consider the electrical circuit presented in Figure 8. It is a basic common mode amplifier, made with one NMOSFET and a resistor.

Let start with the placement of active device: a NMOSFET. A component is added by clicking on **Create/Instance** or the icon  , or hitting the key « i ». The window shown in Figure 9 opens. The component must be found in the proposed libraries. Here, we use the components included in the library **PRIMLIB**.

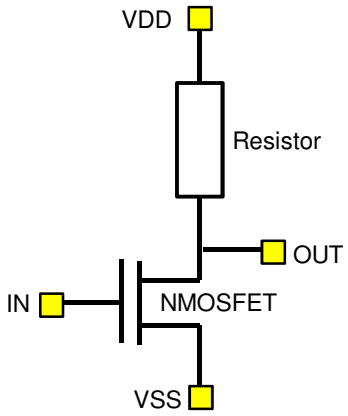

Figure 8 – Basic common-source amplifier

This library contains all the components of the AMS H35 design kit. In the column Category, select MOSFET. Depending on your needs, select one of the following type of N or P-type MOS transistors:

- 20 V for 20 V High Voltage (HV) transistors

- LV-C35 for 3.3 V Low Voltage (LV) transistors
- LV-Isolated for 3.3 V Low Voltage 3.3 V isolated transistors (here, isolated means isolation from substrate noise, which may be a major issue in mixed-signal circuit)

For example, a LV isolated NMOSFET is placed. In the column **Cell,** select the component called **nmosi** (pmosi for a PMOSFET) and the view **Symbol**.

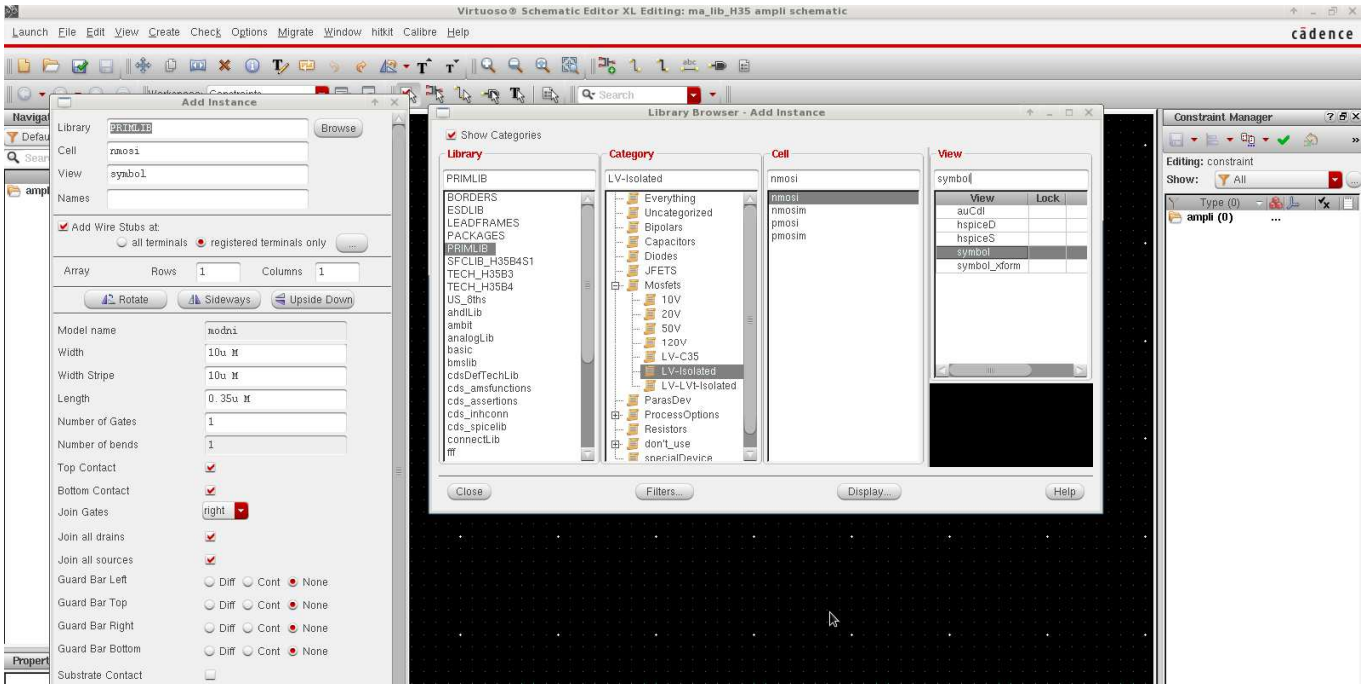

Figure 9 – Add a new component on the schematic diagram

Click on the left button of the mouse to place it and hit the **Esc** key to stop the placement of this type of component.

Design tips:

> When you select any operation on the schematic diagram (e.g. placement or suppression of a component, edition of its properties, etc …), this operation remains active until you hit the key **Esc**. Remember that when you remove one component (key **Suppr**). Once the suppression mode is activated, if you don't hit the key Esc, other components may be deleted if you click on them inadvertently.

> Activate the selection mode to select and edit the properties of components already placed on schematic diagram. Verify that the icon **Default Selection Filter** is activated (the icon is in the bar menu).

> Use the mouse scroll wheel or the arrow of your keypad to navigate on the schematic edition screen. To zoom in or zoom out, click on the commands **Zoom in** or **Zoom out** of the menu **View**, or kit **Alt Gr + [** or **]**.

> The most important shortcuts are given in chapter XII.

Click on the icon **Move** or key m and then select the component to be moved. Its properties can be modified according to one of the following methods:

- Right click on the component and select **Properties** in the pop-up menu

- Key q and click on the component
- Click on the component and modify properties in menu **Property Editor** in bottom-left part of the window Virtuoso Schematic Editor XL

For the NMOSFET which has just been placed, enter the following parameters:

- Model Name : modn
- Width : 150u
- Length : 0.35u
- Number of Gates : 1

These parameters define the transistor model and the geometrical dimensions of its gate respectively. They appear in yellow character close to the component.
Then, a resistor is placed on the drain of the transistor. Click on **Create/Instance (key « i »)** and select the cell **res** in the library **AnalogLib** and the view **Spectre**. This cell view provide the model of an ideal resistor. Call it R1 (property **Instance Name**) and give it the value 100 Ω.
In the next step, a sine waveform voltage generator is added to excite the gate of the transistor. Select the cellview **Vsin** in the library **AnalogLib/Source/Independent** and give it the following properties:

- Name : Vin
- AC magnitude : 1 V
- AC phase : 0
- DC voltage : 0 V
- Offset voltage : 1.5 V
- Amplitude : 100 mV (m for milli)
- Frequency : 100 M (M for MHz)

A DC voltage power supply source must also be placed to bias the transistor: component (**AnalogLib/Source/Independent)** with the following parameters:

- Name : Vdd
- AC magnitude : 0 V
- AC phase : 0
- DC voltage : 5 V

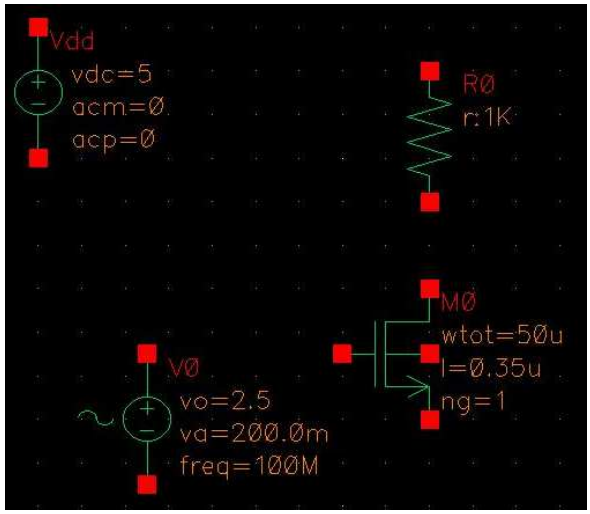

Figure 10 – Placement of the different components of the schematic diagram

Finally, the different component are connected with wires. Click on the icon Wire (narrow)  (key W). Place wire by clicking on each component's terminal that must be interconnected.

Last but not least: a ground reference must be defined in any SPICE schematic diagram. Use the symbol **Global gnd** in the library **analogLib**/**Source**/**Globals**. This symbol will be interpreted as the ground whatever the view. Forgetting the ground symbol will lead to simulation error.

Design tips:

> In a complex schematic diagram, it is recommended to give explicit names to the most important nodes in order to locate signals rapidly Click on the menu Create/Wire Name, or shortcuts L, or click on the icon  .

> For power supply nodes, the global symbol Vdd from the library analogLib can be used.

Once the schematic capture is finished, save and verify it by clicking on the icon **Check and Save**  . Any error will be detected. The faulty symbol will blink and a description of the error will be provided in the CIW window. Figure 11 describes the final result.

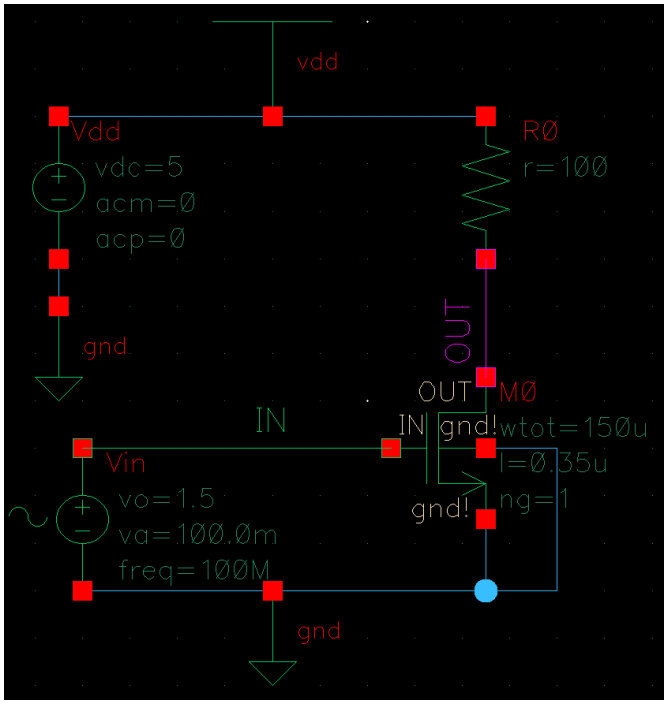

Figure 11 – Final schematic diagram

VII. Launching the results and post-processing of results

1. *Brief reminder on SPICE electrical simulations*

Electrical simulations (e.g. SPICE) aim at computing voltages and current in any points of a complex electrical circuit, and then deducing all the other electrical parameters, such as power, impedance, etc… The simulation is based on a numerical resolution of voltage and current Kirchoff's equations. The purpose of this document is not to detail these numerical methods. For more information, refer to specialized books.
Depending on the used simulator, more or less analysis types are provided. Here, only the three more usual analyses are described, as there are proposed natively by SPICE simulators:

- DC simulation: it is dedicated to the computation of the operating point of a circuit and its evolution according to bias conditions, design variables or temperature. The simulation does not only compute the biasing conditions for one operating point, but for several ones defined by the sweeping of one or two variables (e.g. voltage of bias sources, bias current, design variables, temperature). For example, let suppose that we want to simulate the evolution of the average current consumption according to the power supply voltage. The power supply is modeled by a constant voltage source. DC simulation will sweep the voltage delivered by the source from a minimum to a maximum value. For all the DC voltage, the current will be computed. At the end of the simulation, the evolution of the consumption current will be plotted vs. the power supply voltage. The following table describes the parameters of a DC simulation and the proper syntax.

- Transient simulation (Tran) : it computes the transient response of a circuit (voltage and current waveforms). The convergence of the simulation is dependent on the stability of the simulation circuit. As the behaviour of most of real-case components are non-linear (especially active devices), the simulation duration may become very long. The main parameters of the simulation are the total duration of the simulation time and the step time. Defining excessive simulation time or too small time step would lead to time-consuming simulation. However, there is a trade-off to find between the simulation duration, the accuracy and convergence of the simulation. A too large step time (e.g step time larger than the rising time of an excitation signal) would prevent the simulator to find a stable solution.

- Steady-state frequency simulation (AC) : it is dedicated to the computation of transfer function of circuit in steady-state conditions with small-signal hypothesis whatever the excitation conditions. The behavior of all the components (linear or non-linear) are linearized around their operating point. For non-linear circuits with diodes or transistors, the analysis of the results should be made carefully since the results are valid only if the small-signal assumption is valid. Non-linear effects cannot be reproduced during an AC simulation. In this simulation, all the voltage and current sources deliver sine signals. Whatever the type of sources and the waveform you defined, only the AC parameters of the source will be taken into account and they will be considered as sine generator. The AC parameters are the amplitude and the phase of the sine signal. The frequency is not defined in the source since frequency is swept by the simulator. The simulation parameters define the frequency sweep: the nature of the sweep (linear or logarithmic), the number of points and the min and max frequencies.

Simulation type	Example of SPICE command line	Parameters
DC	.DC Vs1 min1 max1 step1 .DC Vs1 min1 max1 step1 Vs2 min2 max2 step2	• Vs1 and Vs2: primary and secondary parameters or sources • Min1, max1 : min and max boundaries for the primary parameter • Min2, max2 : min and max boundaries for the secondary parameter • Step1, Step1 : step for primary and secondary parameters
Tran	.TRAN step tstop (tstart)	• Step: step time for the simulation • tstop: stop time for the simulation • tstart: start time for the simulation (optional)
AC	.AC typ step fstart fstop	• Typ: frequency sweep type. LIN = linear sweep, DEC = logarithmic sweep • step: if Typ = LIN, number of points

		between fstart and fstop. If Typ = DEC, number of points per decade • fstart : min frequency. • fstop : max frequency

Figure 12 – Summary of the main parameters of the three basic SPICE's simulations

Design tips: Units

Writing the units of physical variables is not necessary. For example, if you define the amplitude of a votlage generator to 1 V, don't write « 1 V », but « 1 » directly. The unit is implicit. Similarly, if you define the capacity of a capacitor don't write « 1 pF », but « 1e-12 » or « 1p ».
Use the prefix milli-, méga, giga … to precise the decade. The syntax is:

- 1e-15 : femto (f)
- 1e-12 : pico (p)
- 1e-9 : nano (n)
- 1e-6 : micro (u, not µ !)
- 1e-3 : milli (m)
- 1e6 : méga (M, m for milli !)
- 1e9 : giga (G)

2. General methodology to set-up a simulation with Analog Design Environment XL

Now, the circuit's schematic built in VI will be simulation with the Cadence simulator SPECTRE. From Virtuoso Schematic Editor, click on **Launch**/**ADE XL**, select **« Create new view »** and use the on-going schematic.
A new tab in created in the window **Virtuoso Analog Design Environment XL**, as presented below: this is the environement ADE (G)XL. It will be used to define all the simulations, variables and parameters associated to the schematic diagram. From this window, the schematic diagram will be modified (tab Virtuoso Schematic Editor), the simulation will be configured, launched and the results analyzed (tab ADE XL)

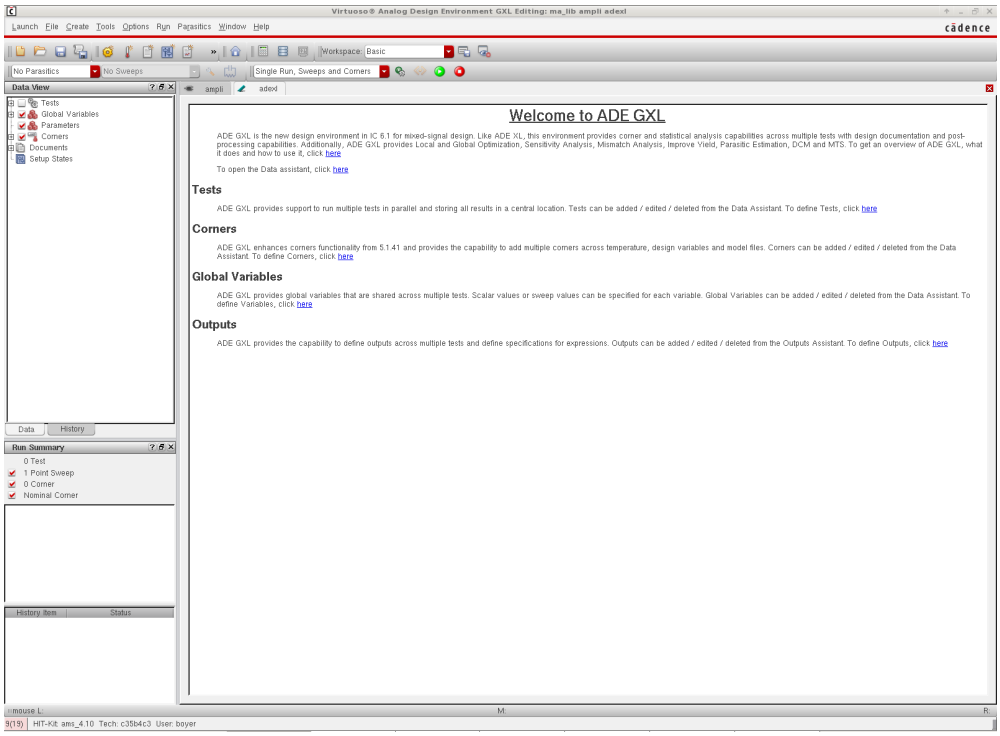

Figure 13 – ADE (G)XL – Simulation environment

The menu **Data View** in the top left corner lists all the simulations (Tests), variables, parameters and corners (see part X) associated to the schematic diagram. The first time you will use ADE GXL, it will be complex and unclear because of the large number of menu. To get familiar with this tool, we start with a simpler method to configure simulations from the tool ADE XL. With more experience about the simulation and result analysis process, you will be able to manage all the simulations with ADE GXL.

ADE XL is launched when a new Test is created. Click on **Create/Test** or on the icon  . Note that a new test may also be created from the menu Data View by clicking on Add Analysis. The window below opens. The selected simulator is Spectre, as shown on left bottom corner of the window. The default temperature for simulation is 27°c: remember that temperature has a huge influence on device performances.

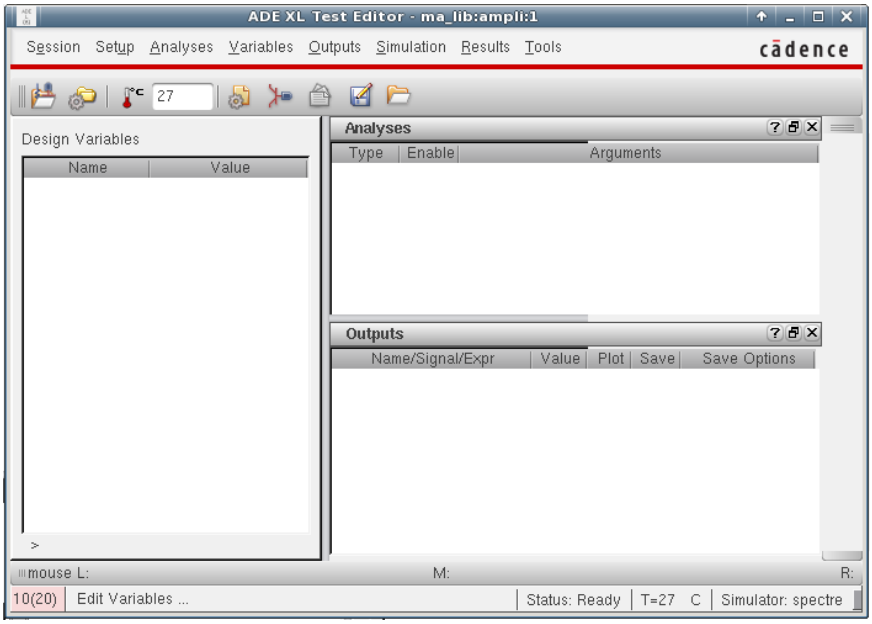

Figure 14 – Virtuoso Analog Design Environment – Launching the simulator SPECTRE

Click on **Setup/Model Libraries** to show the access path of used libraries (Figure 15). The library that contains MOSFET models of AMS H35 design kit is cmos53.scs. The column section indicates the default section of the library used for the simulation. The sections define the model's parameter for different technological process conditions (see part X. corner analyses). TM means Typical Mean, i.e. typical values for the technological process parameters.

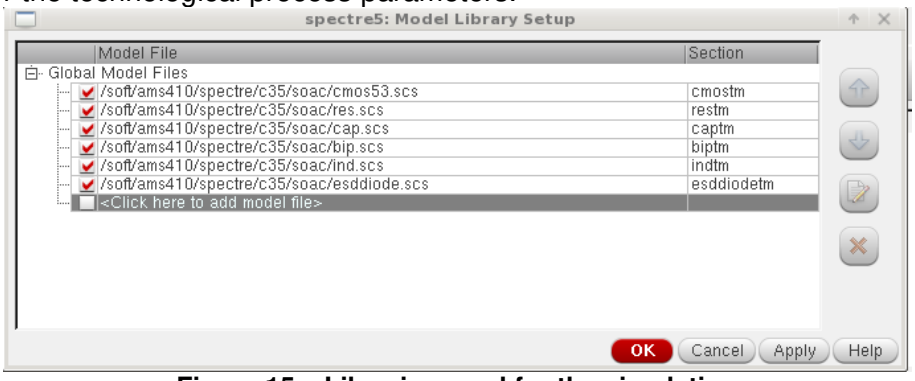

Figure 15 – Libraries used for the simulation

3. *Transient simulation*

Transient simulations aim at computing the response of a circuit in time domain from initial conditions. First, click on **Analyses/Choose** to add a new simulation profile. The window shown below opens. In the field **Analysis**, select tran and set the parameter Stop Time to 100 ns (maximum simulation time). Check the box **Enabled** to activate this new simulation profile. Each time a simulation will be launched, simulations associated to this profile will be launched automatically. Click on OK to validate. The new simulation profile is now visible in the window **Virtuoso Analog Design Environment**. If you click on this profile, you can modify the simulation parameters.
SPECTRE proposes several types of simulation:

- Tran : transient
- Dc : DC analysis
- Ac : AC analyse
- Noise : noise analysis (AC analysis)
- Sp : S parameter analysis (AC analysis)

Select transient simulation and configure the simulation time (Stop time). To set more parameters, click on the button **Options**. Click on OK to validate.

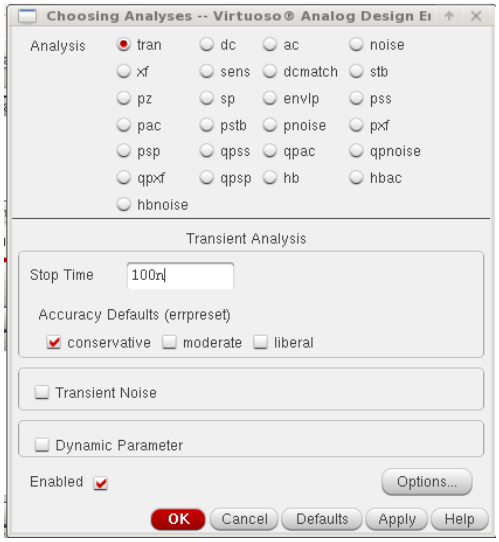

Figure 16 – Setting the parameters of a transient simulation

Then click on **Simulation/Debug Test** to generate the circuit netlist. A netlist is a file that describes the topology of the circuit, as a graph where every components are interconnected by nodes. A new window Output Log opens to show the state and the progression of the simulation. The success of the

simulation is also indicated in the CIW window. The netlist file can be opened by clicking on **Simulation/Netlist/Display**.
To display and post-process simulation results, click on **Results/Direct Plot/Transient Signal**. The window **Direct Plot Form** opens. You can select voltages and currents to be plotted on the schematic diagram directly. For example, click on the wires (a wire is actually a node in the netlist) connected to the gate and drain of the MOSFET (input and output of the amplifier) and then hit the key Esc. The result is displayed, as shown in Figure 17. In the menu on the right part of the window, you can select the curves to be displayed or deleted, or change the color of the curves. Placing the mouse cursor over a curve shows the point coordinates. Markers can be added on the graph by clicking on the icon  .

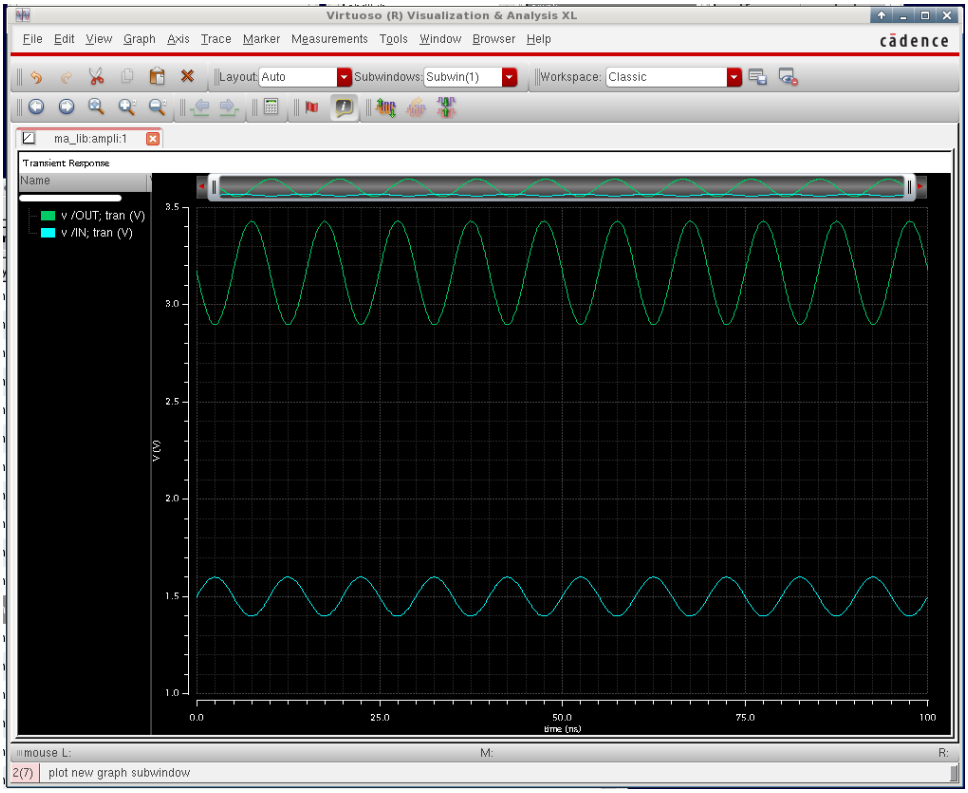

Figure 17 – Plot the result of a transient simulation

Click on **Tools/Calculator**, to open the tool Calculator. It is dedicated to mathematical operations on simulation results. Part VII.6 provide more details about this tool.

Selection of the results to display before the simulation

The results to be displayed can be selected before launching the simulation from the ADE XL window.

In **Outputs Setup**, click on the icon **Add new output**  to add new signals (voltage and current) or expression. A new line is added on the displayed output table. Provide the name of the signal in the column **Name**. In the column **Expression/Signal/file**, double-click in the blank field and the button **Select from Schematic**  appears, in order to select a node (voltage selection) or a device terminal (current selection).

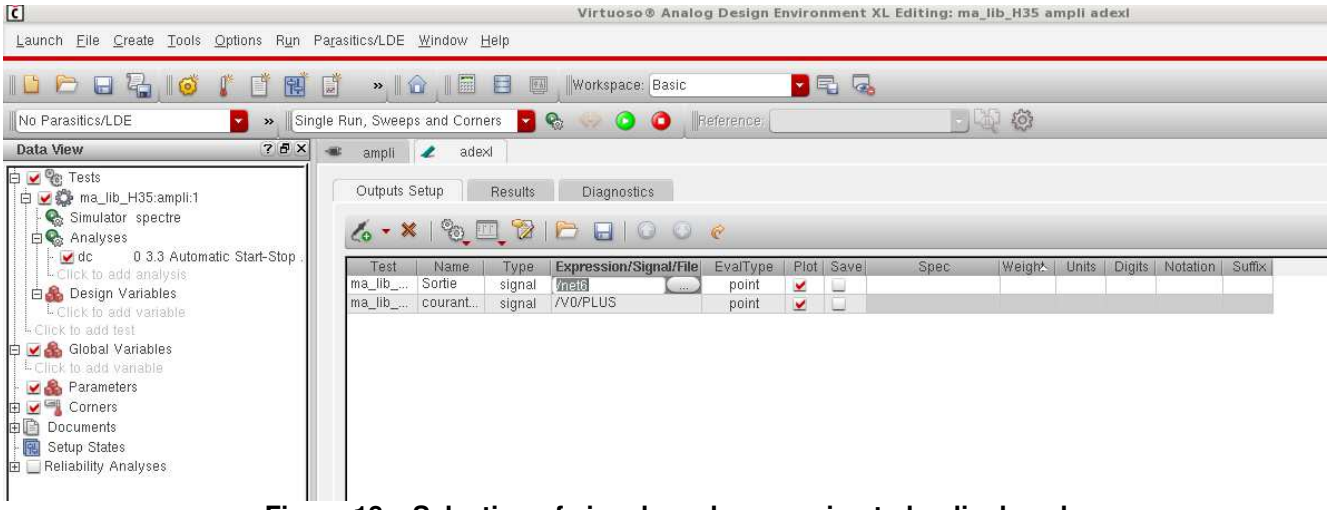

Figure 18 – Selection of signals and expression to be displayed

4. DC simulation

Then we perform a DC simulation to compute the evolution of the operating point of the transistors according to the gate voltage. First, add a new simulation profile by clicking on **Analysis**/**Choose**. Select **DC**: numerous parameters can be swept, such as component temperature (junction temperature for bipolar, MOSFET or diodes), a global variable, a component or model parameter. Here, we want to sweep the DC voltage of the gate excitation source. Select **Component Parameter**. Select the component (the voltage source Vin) directly on the schematic diagram by clicking on the button **Select Component**. The window shown below opens with all the parameters of this component. Select the parameter dc and click OK. Then, define the sweep type:

- Start – Stop : from 0 to 5 V
- Sweep Type : Linear, Step Size = 0.1

Click on OK to validate the DC analysis. In the window **Virtuoso Analog Design Environment**, in the column **Analyses**, two simulation profiles are now visible and active (filed **Enable**). To modify them, click on one of them. Deselect **Enabled** to deactivate one of them.

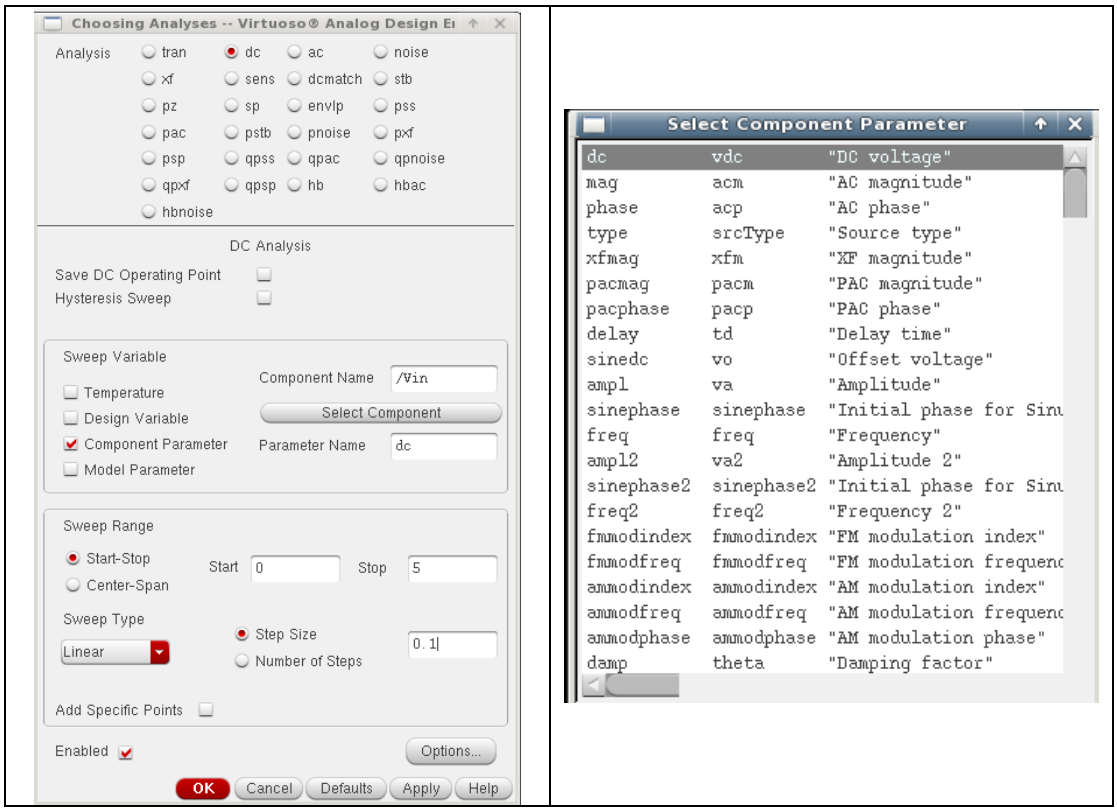

Figure 19 – Setting the parameters of a DC simulation

Launch the simulation. Once it is achieved, display the results by clicking on **Results/Direct Plot/ Main Form**. The window shown below opens.

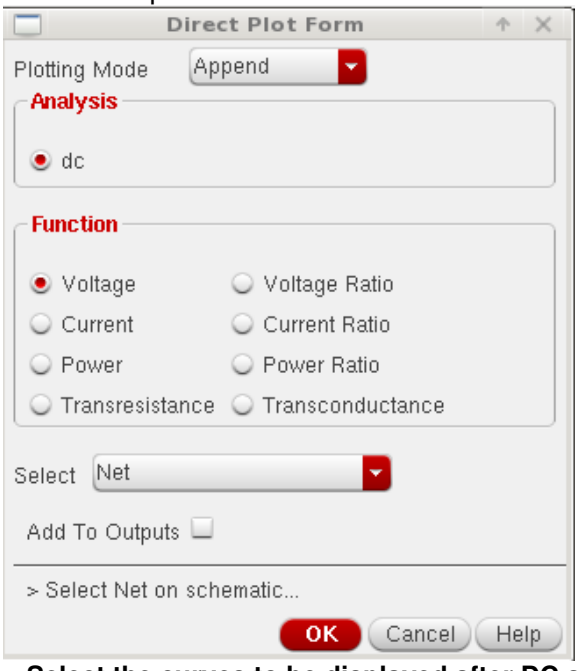

Figure 20 – Select the curves to be displayed after DC simulation

In this window, the results of the different analyses can be selected and plotted. For example, select DC analysis. Select the function: **Voltage**. Specify the representation mode: single-ended (**net**) or differential mode (**Differential Nets**). Finally, select the node directly on the schematic diagram: the input and output nodes in this example. Each time you click a node on the schematic diagram, a new curve is plotted. Figure 21 shows the final result after the DC analysis and the selection of the input and output nodes. Properties of the curves can be changed by clicking on them.

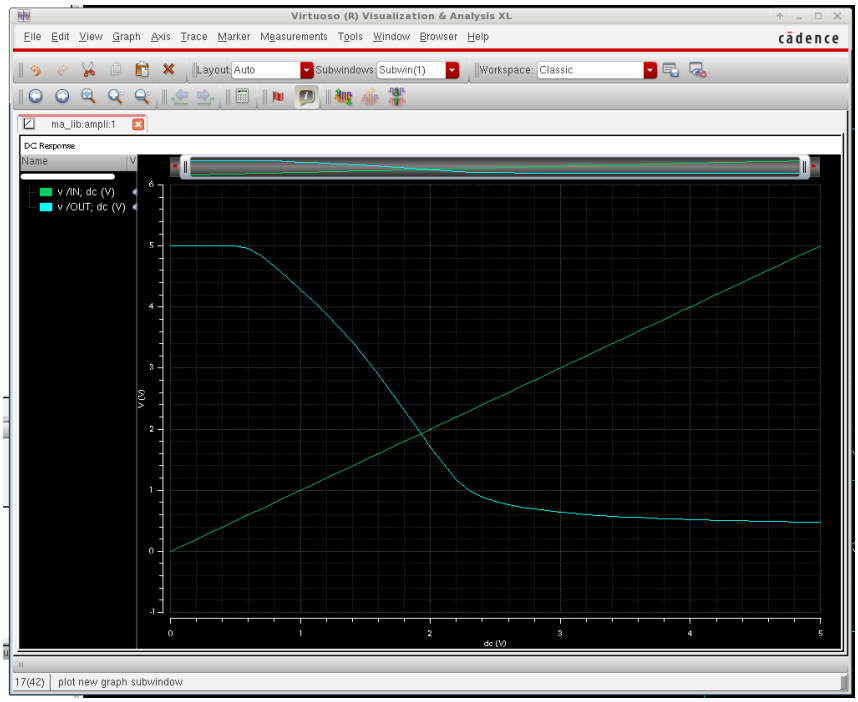

Figure 21 – Plot DC simulation results

Then, we decide to open a second graphical window to plot the evolution of the bias current of the amplifier. Click on **Results/Direct Plot Form/New Subwindow** in **Plotting Mode**. In the window **Direct Plot Form**, select **Current** and **New SubWin** in the option **Plotting Mode**. Don't select node but device terminals to plot current. In the schematic diagram, click on the terminal of the power supply voltage generator. The result is shown below.

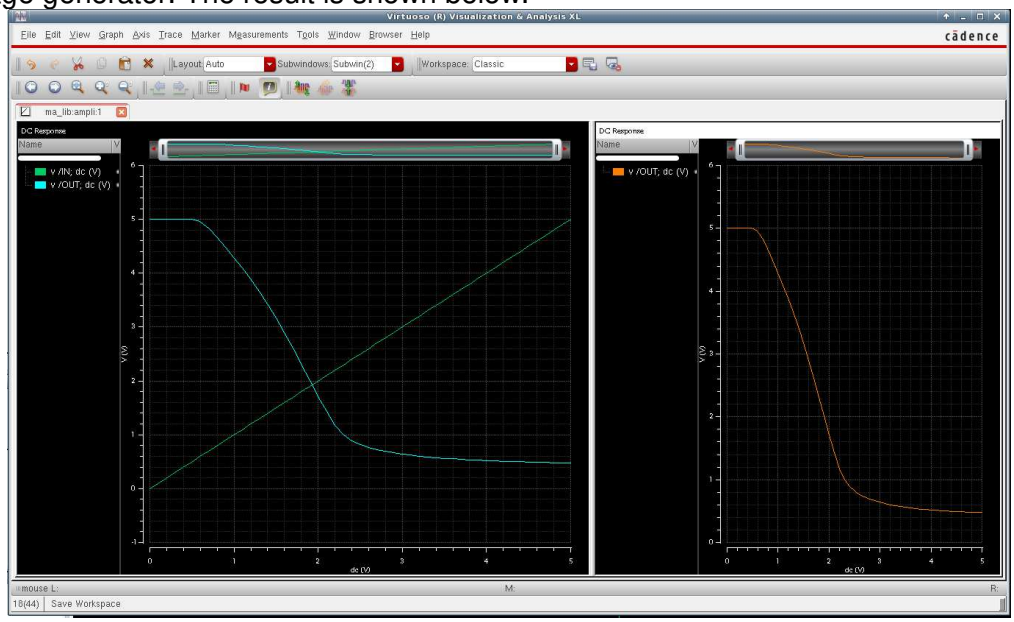

Figure 22 – Plot DC simulation results - Add a second subwindow

Design tips: Save session parameters

You can save the parameters of the different analyses launched during a session. Click on **Session/Save State** and give a name to the state of your session. They will be reloaded the next time **Virtuoso Analog Design Environment** will be opened by clicking on **Session/Load State**.

5. AC Simulation

We perform now an AC simulation in order to compute the transfer function between the output and the input of the amplifier stage. The first verification consists in checking the configuration of all the voltage and current sources in the schematic diagram. Only the AC parameters will be taken into account during the AC simulation. As we want to compute the transfer function from the input to the output of the amplifier, only the input generator must excite the circuit. Its AC amplitude must be different to 0, in contrary to all the other sources. For example, if the power supply generator has also an AC amplitude different to 0, it will also excite the circuit. Thus, the simulation will compute the response of the circuit when two sinusoidal excitations are applied: one on the input node, the other on the power supply.
The parameters of the input voltage source Vin are modified by editing its properties (Figure 23). two parameters are taken into account during AC simulation (they are ignored in DC or transient simulations):

- AC magnitude: it specifies the amplitude of the source during the AC simulation, whatever the frequency. It is advised to select 1 V since the simulation result will give the transfer function directly.
- AC phase: it specifies the phase of the source during the AC simulation, whatever the frequency.

Design tips: DC parameter during AC simulation

Before any AC simulation, SPICE simulators perform a DC simulation to determine the operating point of the circuit under test. AC simulation is based on the assumption that the circuit is linear around the operating point. Therefore, you have also to verify the DC parameter of the different voltage and current sources to ensure that your simulation is done with the correct bias conditions.

Then, define a new simulation profile by clicking on **Analysis**/**Choose**. Select **AC** and define the sweep type :

- Sweep variable : Frequency
- Start – Stop : from 1 MHZ to 10 GHz
- Sweep Type : Logarithmic, Points Per Decade : 100

Check the box Enabled et click on OK to validate the AC analysis.

Figure 23 –AC parameters of a voltage source

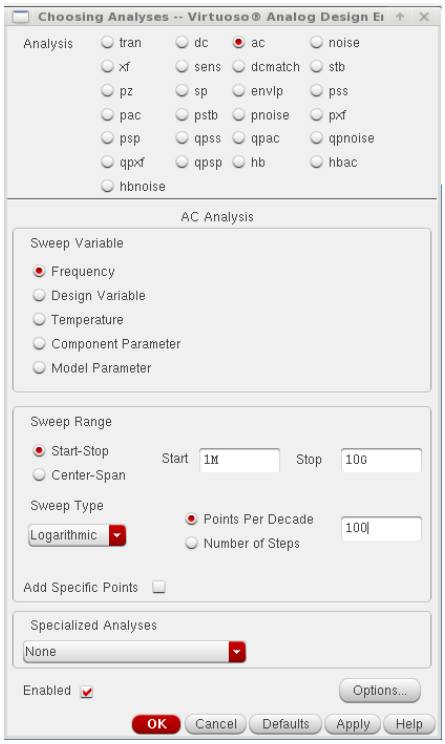

Figure 24 – Configuration of an AC simulation

Launch the simulation. At the simulation is achieved, click on **Results**/**Direct Plot**/ **Main Form** to plot the results. The following window opens. Select the option dB20 to plot the module of the transfer

function in dB. Then, add a new subwindow to plot the phase. The plot of the transfer function of the amplifier is presented below.

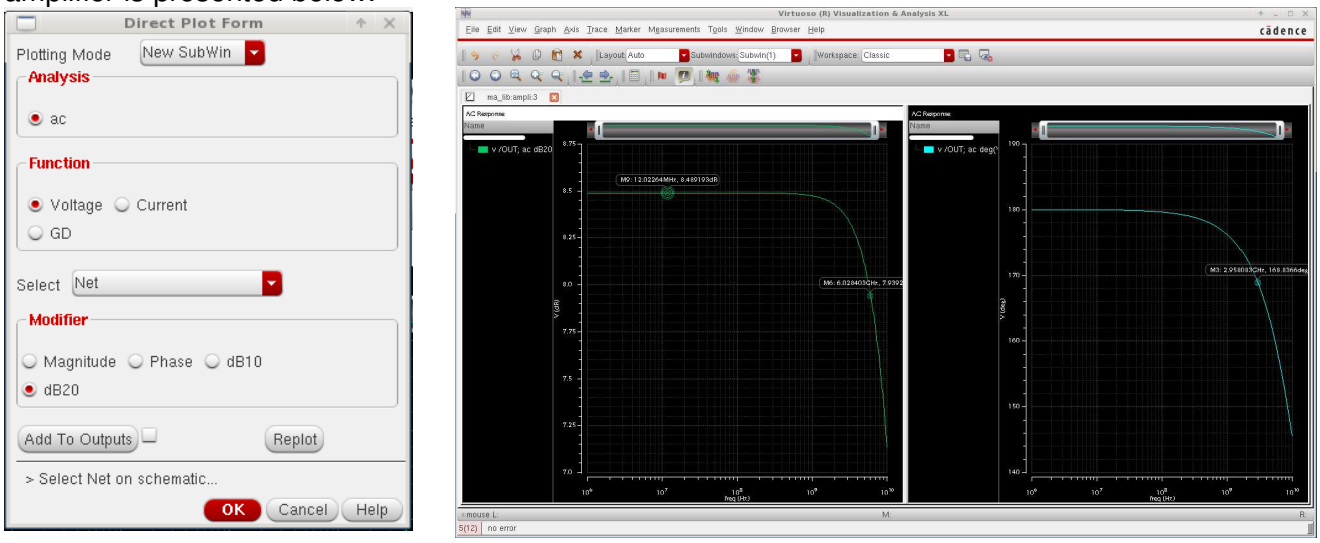

Figure 25 – Plot of the transfer function of the amplifier computed with an AC simulation

6. *Mathematical operators*

Only the main electrical parameters (voltage, current, power, transconductance, S parameters…) may be plotted from the window **Direct Plot Form**. In order to plot more parameters, it is necessary to compute mathematical expressions based on the plotted variables. It is possible with tool Calculator.
In order to illustrate it, let consider the example of the DC simulation (VII.4). Here, we want to express the plotted voltage in dBV. Launch the DC simulation and plot the DC voltage on the output node of the amplifier. From the ADE XL window, click on **Tools/Calculator** or in **Output Setups**, add a new expression and click in the field **Expression/Signal/File** to open the tool Calculator.
Figure 26 opens. A calculator with a large set of mathematical function is provided.

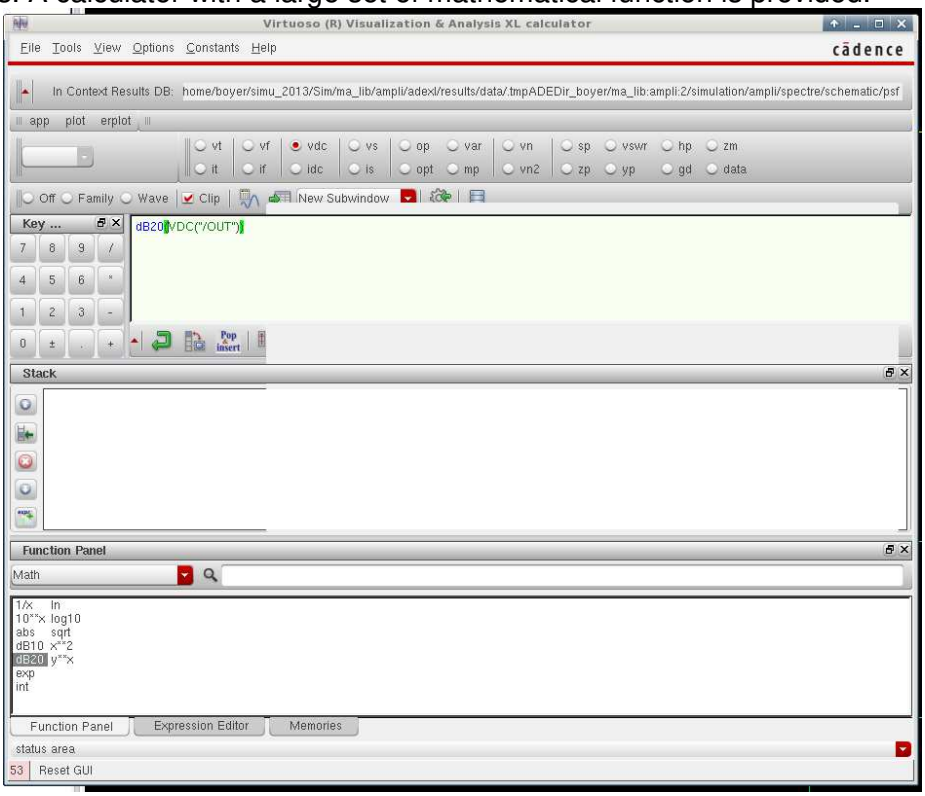

Figure 26 – Tool Calculator

Functions are available in the panel **Function Panel** (in the bottom part of the tool Calculator). First, select the waveform or the node, then apply the function **dB20**. Check the box **vdc** (voltage computed by a DC simulation) and select the waveform by clicking on the plotted curve. The selected voltage appears in the command line of the calculator. Click on **dB20**, and on **Tools**/**Plot** or the icon to plot the result.

Click on the icon to export the waveform in an Excel file. Click on the icon to add this expression in the expressions saved in the ADE XL session.

Many other functions are provided by this tool. They are not detailed in this document. You may consult the on-line help of Cadence for more information. This on-line help is available from AIME. The following table summarizes the most usual function for signal analysis purpose.

Operator	**Function**
mag	Magnitude
phase	Phase
real	Real part
imag	Imaginary part
ln	Natural logarithm
log10	Base 10 logarithm
dB10	Base 10 dB (for power)
dB20	Base 20 dB (for voltage or current)

The table below lists some advanced function which should be useful for your project.

Operator	**Function**
average	Average value of a signal
bandwidth	Compute the bandwidth of a signal
compression	Value at 1 dB compression point
dBm	Compute the power in dBm(W)
dft	Discrete Fourier transform
FourierEval	Fourier transform
frequency	Extract the frequency of a periodical signal
rms	RMS value of a signal

Design tips: Compute expressions

You can define mathematical expressions made on simulated parameters before launching the simulation. During the output selection (**Add new output**), select Expression instead of Signal. The tool Calculator will open to define the mathematical expression.

VIII. Create a symbol

Large circuits are made of thousands or millions of transistors, gates and elementary structures. Schematic diagram with only elementary components (MOS devices, capacitor, resistor, bipolar junction transistor, etc…) may become extremely difficult to read. In practice, it is better to use hierarchical design, i.e. the circuit is subdivided in several subparts or subcircuits, which appear as

individual symbols. Their schematic diagram is defined within this symbol. Moreover, each part of the circuit can be validated independently and then assembled to form the final circuit.
Let use the amplifier example to illustrate the construction of a symbol. From the window **Virtuoso Schematic Editor XL**, click on **File/Save a copy** and save it as ampli_symbol. You can close the window with the view ampli, and open a new view from Library Manager..
On the new schematic, remove all the voltage generators used as stimuli for simulations. They are not part of the physical circuit. I/O pins have to be placed at the terminals of the subcircuit (input, output, power supply, bias reference, etc…). Click on **Create/Pin** or hit the key « P » to add an I/O pin. A window opens to specify the name of the I/O pin and its direction (this parameter changes only the graphical symbol of the pin). Create the pins In and Out. Add Vdd and Vss. Figure 27 shows the schematic diagram used to generate the symbol of the amplifier.

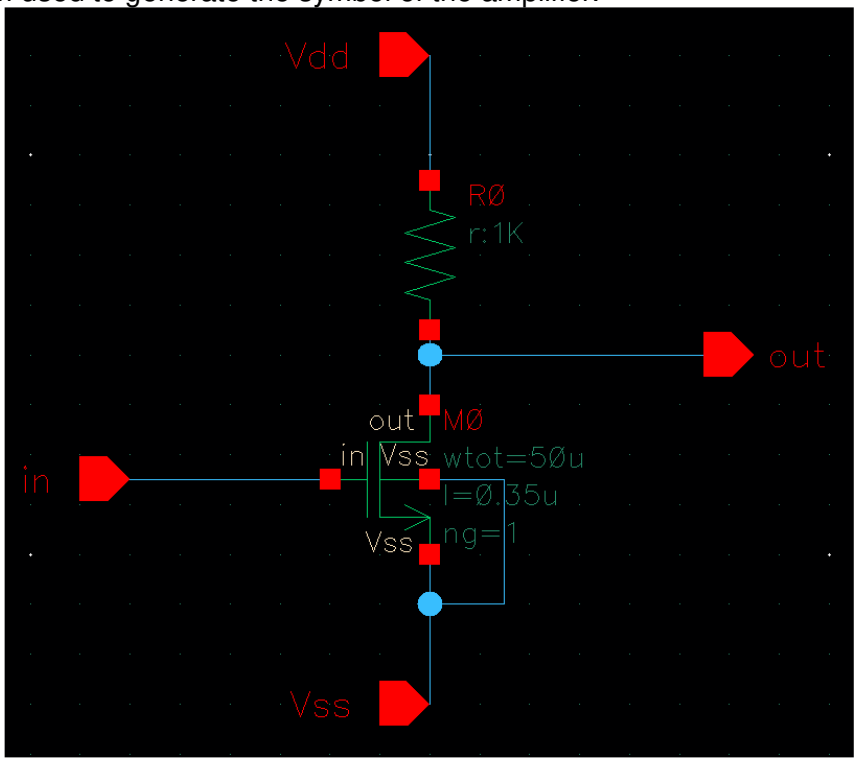

Figure 27 – Schematic diagram used to generate the symbol of the amplifier

Click on **Create/Cellview/From cellview …** The following window opens. Specify the name of the library, the cell and the view (ampli_symbol) and click on **Apply**.

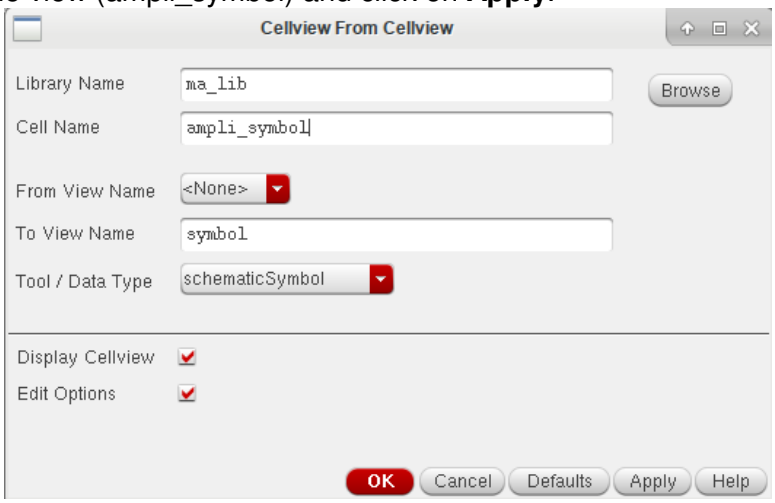

Figure 28 – Create a new symbol from a schematic diagram

The window **Symbol Generation Options** opens to adjust the positions of the I/O pins and the shape of the symbol (right, left, top or bottom). Click on OK. The symbol is generated automatically and

appears as a rectangular box with the four I/O pins defined before (Figure 29). You may save the symbol and close the schematic diagram.

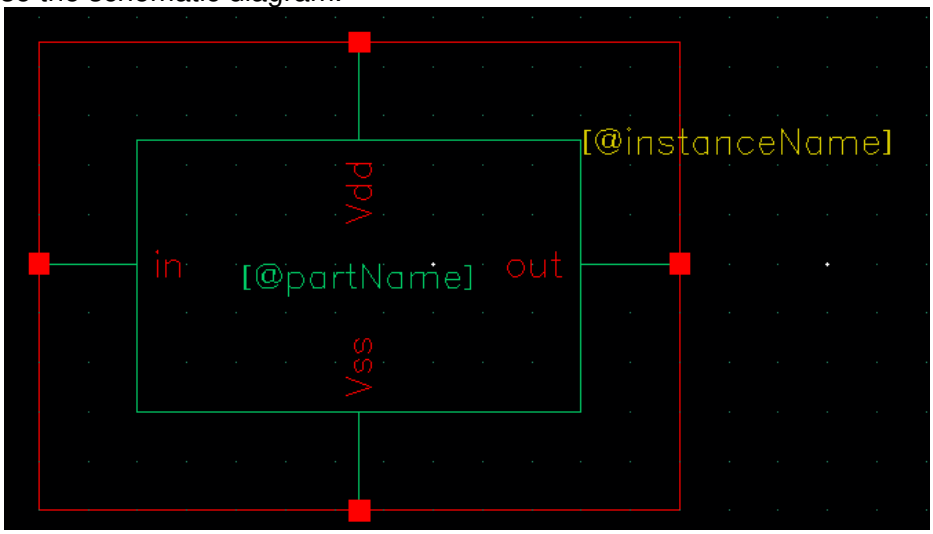

Figure 29 – Symbol of the amplifier

Now, this symbol will be used in another schematic diagram to simulate the amplifier. Create a new schematic called ampli_simu and open it the schematic editor Virtuoso. Ajoutez a DC voltage generator and a sine voltage generator (library analogLib) and the symbol ampli_symbol (ma_lib). Connect the different components as shown below.

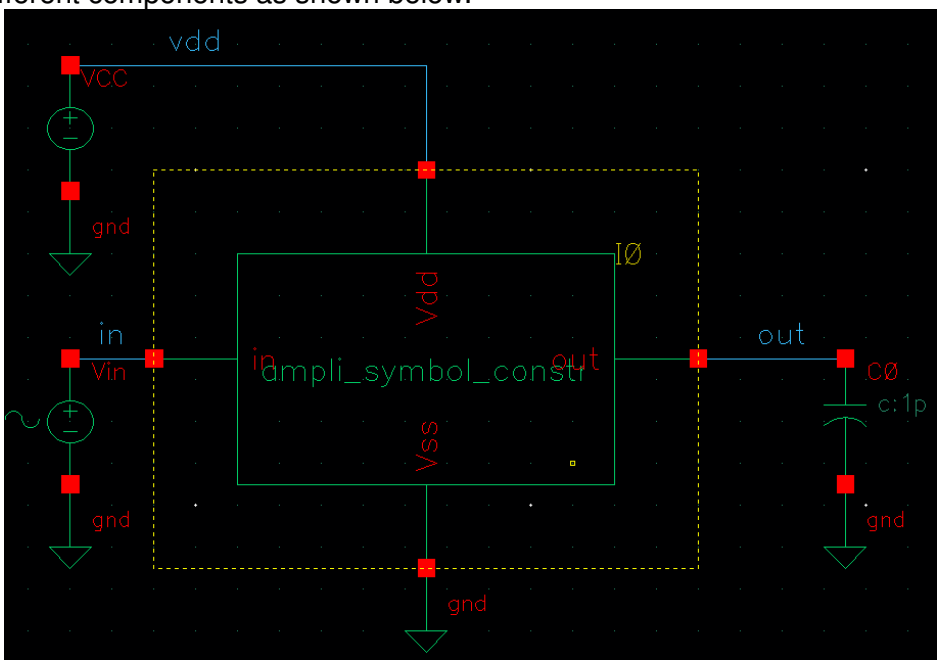

Figure 30 – Schematic diagram to simulate the amplifier

Save this new schematic diagram and check the errors. You can load the previous simulation sessions in order to launch the simulations performed in the previous parts.

Design tips: Descend into hierarchy

Designing with high level symbol that describes a functional block is a typical practice in circuit design. This symbol is also called subcircuit in SPICE syntax. A subcircuit can be made of several subcircuit. Hence, the schematic diagram can contain a multilevel hierarchy of symbol and subcircuit. Descending in the hierarchy means opening the schematic of a subcircuit included in a circuit diagram.

To descend into the hierarch, click on the menu **Edit/Hierarchy/Descend Edit (Shift+E)** or **Descend Read (E)**. The window **Descend** is opening in order to select the type of view to open (e.g. Schematic) or the type of reading (edit, read). You can also click on the symbol.
In order to ascend into the hierarchy, click on the menu **Edit/Hierarchy/Return (Ctrl+E)** or **Return to Top**.

IX. Parametric simulation – Plot the Ids(Vds,Vgs) static characteristic of a MOS transistor

The goal of a parametric simulation is to observe the influence of one or several parameters of the model (e.g. a resistance, the length of a gate, the bias voltage of an analog circuit, etc…). It consists in sweeping the values of these parameters and iterate the simulation for every parameter value. At the end of the simulations, the evolution of circuit's performances may be plotted vs. the parameter values.
Parametric simulations is required to plot the static characteristic Ids(Vds,Vgs) of a MOSFET. This characteristic is extremely valuable to determine the threshold voltage of a MOSFET, its maximum drain current at saturation, or the voltage drop between drain and source for a given channel current. In practice, the transistors of an output buffer are dimensioned such that they can deliver (or absorb) a maximum current with a certain voltage drop Vds.
In this part, we will illustrate the configuration of a parametric simulation with the example of the static characteristic of a MOSFET. Let consider the NMOSFET used in the amplifier example. Figure 31 shows the schematic diagram used to extract the static characteristic. Two DC voltage generator are connected on the gate and the drain of the MOSFET. The source and the minus terminals of the generators are connected to the same reference (ground). By default, the DC propertie of both generator is set to 1 V.

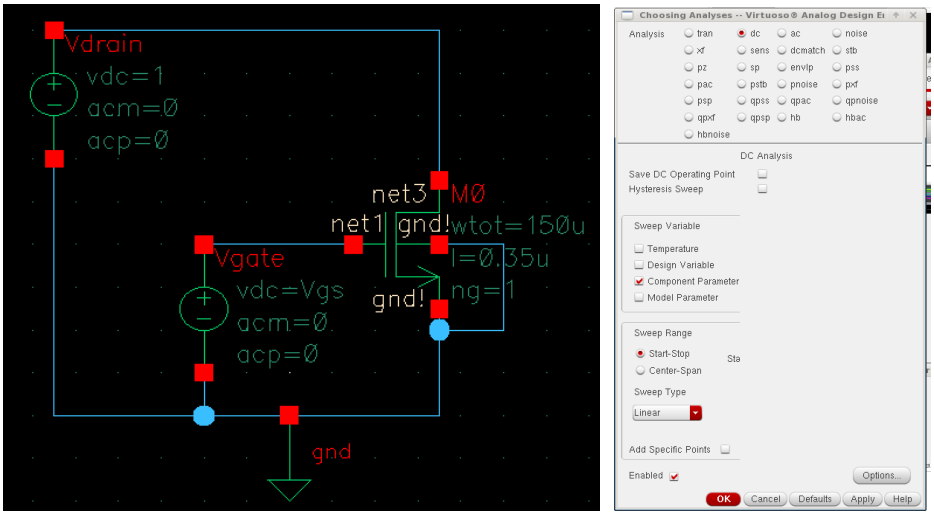

Figure 31 – Schematic diagram to simulate the static characteristic of a NMOSFET

A DC simulation is required since the static characteristic shows all the operating points of the MOSFET for the different drain and gate biasing conditions. For example, the voltage Vds can be used as sweeping variable of the DC simulation (see Figure 31 for the DC simulation configuration). At the end of the simulation, we could plot the evolution of the drain current vs. the drain voltage, but only for one gate voltage value !

We have to pass the DC voltage of the generator Vgate as a model parameter. First, create a global variables which is related to the DC voltage of the generator Vgate. Open the properties of the source Vgate. Fill the field Vdc with the variable name "Vgs" (or any other name). Vgs will be the variable that will be used to sweep the DC voltage of the generator Vgate during simulations.
In the ADE XL window, this variable has to be declared. In the menu **Data View**, under **Global Variable**, click on **Add variable**. Specify the name of the variable in the field 'Variable Name' and its value in 'Variable Value'. Click on OK to validate (Figure 32). The next time a simulation will be launched, the specified value for the variable Vgs will be considered.

Figure 32 – Declaration of a global variable

However, it is necessary to sweep different values of Vgs to plot the Ids(Vds;Vgs) characteristic. In the menu **Data View**, edit the variable Vgs. The following window opens to configure the type and the extend of the sweep of the variable Vgs (e.g. from 0 V to 5 V with a constant step equal to 1 V). Select Exclusion to not include the default value of the variable in the simulation list.

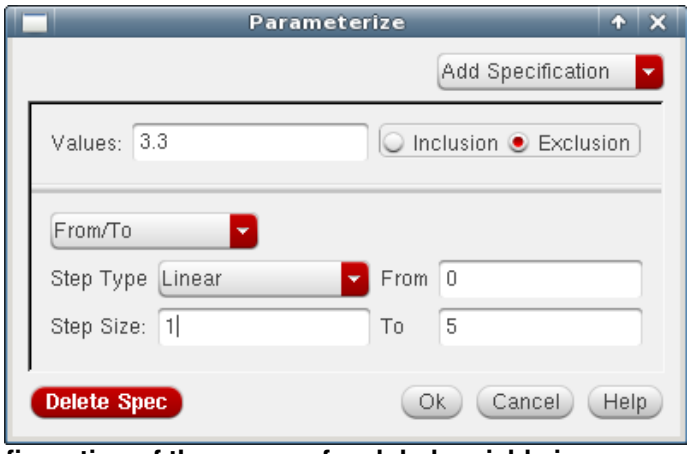

Figure 33 – Configuration of the sweep of a global variable in a parametric simulation

Finally, click on the button  to launch the parametric simulation. The simulations defined in the session will iterate N times, where N is the number of values taken by the swept variable. If you have defined several variables, be careful in the number of iteration since the simulation duration may become excessive rapidly.
At the end of the simulation, select one terminal of the generator Vdrain to plot the drain current (**Results/Direct Plot/Main form**). Several curves are plotted. Each curve is associated to one gate voltage value. The result is shown in Figure 34.

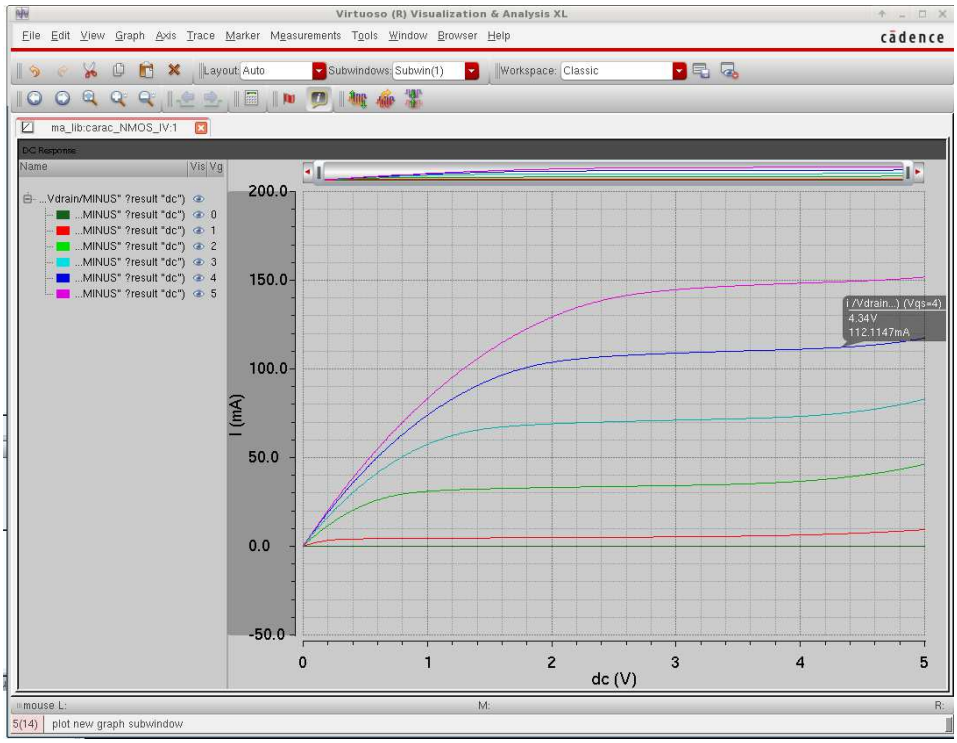

Figure 34 – Result of the parametric simulation – Plot of the static characteristic of a NMOSFET

X. Simulation of the temperature

The performances of electronic components (especially MOS devices) are temperature dependent. That's why circuit's performances must be simulated at different temperature. In SPICE simulator, there is a global variable that control the temperature. This temperature is the junction temperature, i.e. the temperature within each component. This temperature is supposed constant in all the component of a schematic diagram. By default, the temperature used by SPECTRE simulator is 27°c.
The temperature can be changed in the window ADE XL by right-clicking on the menu **Data View**. Select **Temperature** to open the window shown in Figure 35.

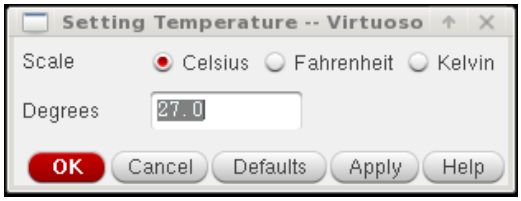

Figure 35 – Modification of the simulation temperature

In practice, electronic circuits must operate satisfactorily over a more or less large temperature range. For example, most of commercial electronic product must operate on the range 0 - 80°c. Automotive or industrial products have usually to operate on the range -40°c - 150 °c. In simulation, it is recommended to simulate the performances of a circuit at several temperature spread over the specified temperature range (for example from -40°c to 120°c by step of 40°c).
The temperature can be changed manually or with a parametric simulation (see part IX). For example, let consider the static characteristic of the MOSFET studied in part IX. We want to simulate the influence of the temperature on the maximum saturation current of the MOSFET. We will remove the

parameter Vgs and replace it by the temperature (it is possible define two parameters but the results will show the influence of both the gate voltage and the temperature). Set the DC voltage of Vgs to 3.3 V.
In the menu **Data View**, create a new variable **temperature**. Right-click on it to edit its properties and define the sweeping: for example 3 temperature points between 0°c and 80°c. The result of the parametric simulation is shown in Figure 36. It confirms that the increase of the temperature leads to a significant decrease of the saturation current.

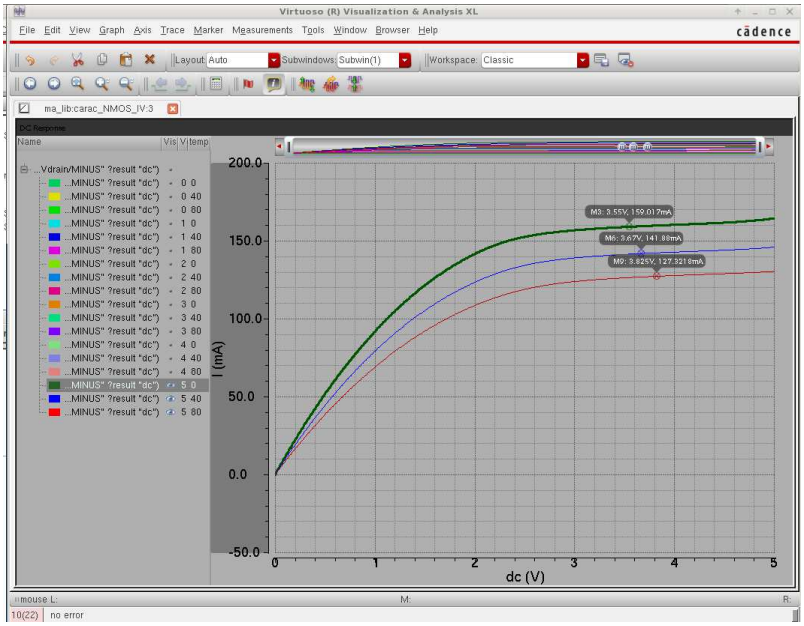

Figure 36 – Simulation of the influence of the junction temperature on the drain current of a MOSFET

XI. Corner analysis

Up to now, simulations have been done with the component models of design kit AMS C35 in typical process conditions. This typical process conditions mean that the values of the model parameters take the average values of the fabrication process. However, it is an ideal case. In practice, geometrical and physical parameters of any components are not perfectly controlled and vary randomly: this effect is called process variation. For example, if you design 100 NMOSFET with a given gate length on the same die or on different dies, these 100 NMOSFET will not have exactly the same gate length.
These variations may lead to a dispersion of the performances of a circuit, which has to be controlled and limited by the manufacturer to optimize a sufficient yield. In simulation, it is possible to simulate the influence of process variations and verify that the performances of the circuit are not dispersed too much. However, there is an infinite number of configurations to simulate in order to obtain the statistical distribution taken by circuit's performances. One industrial and efficient method to tackle this problem is called Corner Analysis. It consists in simulating the circuit's performances only in the worst case conditions, or corners. AMS C35 design kit provides the models of the components not only in typical process conditions, but also in worst-case process conditions (i.e. when component's parameters take extreme values).

However, there are two other sources of variability of circuit performances:

- temperature
- power supply voltage

In practice, the analysis of process variation is coupled with the analysis of temperature and power supply voltage variations. A corner analysis is also used, so that simulations will be done for extreme values of temperature, power supply voltage and process parameters.

To configure a corner analysis, return to the CIW window and click on **HIT-KIT Utilities/Simulation Utilities/Corner Analysis**. The following window opens.

Figure 37 – Configuration of a corner analysis

The access path for the models of the AMS components is given by **Path to Models**. The default access path is: /soft/ams410/spectre/h35/soac. In case of simulation problems, change the access path to: /soft/ams410/spectre/h35.
The first part of this window specifies the process corners: the type of components (MOSFET, BJT, resistors…) that will be used in the process corner analysis are selected. In Figure 37, only the box cmos53 is checked, so process corner analysis will affect only the MOSFET parameters. The library cmos53 (c35) contains different sections which are associated to the different process corners :

- Tm : typical mean (typical process conditions)
- Ws : worst-case speed (process conditions that lead to the slowest transition in a digital gate)
- Wp : worst-case power (process conditions that lead to the fastest transition in a digital gate but also to the maximum power consumption)

By default, all the corners are selected. Click on the button Change to remove or add corners.
The two next parts concern temperature and power supply voltage (Vsupply) corners. Similarly, click on Change to modify the list of corners. In practice, select one typical value, a minimum and a maximum value.
Click on the button **Edit corners** to show the list of all the selected corners (Figure 38).

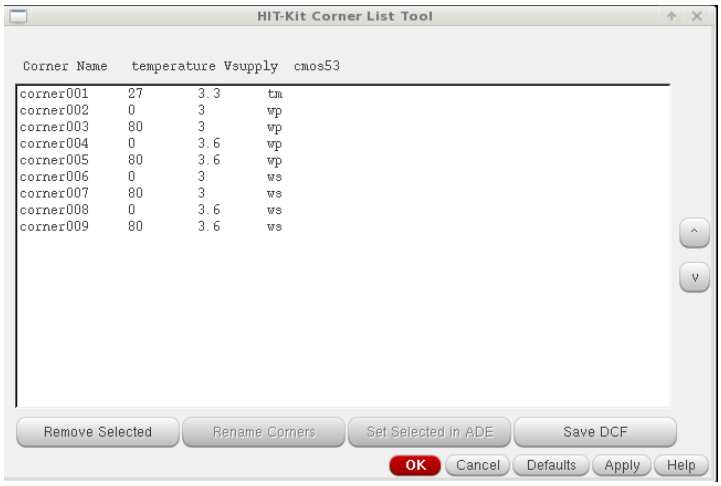

Figure 38 – List of selected corners

Save the corner list in a .dcf file. Click on the button **Save DCF As…,** select the directory with the pop-up window and type the name of the file in the field **Corners File**. Click on **OK** and **Close.**
Go back to the window ADE GXL. In the menu top left part of **Dataview**, all the tests, variables, parameters, corners associated to one schematic diagram are visible. Double-click on it to edit the properties.
First, the simulations to perform have to be configured. As the parametric analysis, the corner analysis only change model parameters and launch the simulator iteratively. Once the simulation is configured, click on **Create**/**Corner** or on the icon  or on Corner in the menu **Dataview**. The window below opens, with only one default corner (nominal voltage, temperature, typical mean process). Import the .dcf file which contains the list of corners. All the corners are loaded. Select the corners that you want to simulate and click on OK. The temperature and voltage values may be changed from this screen.

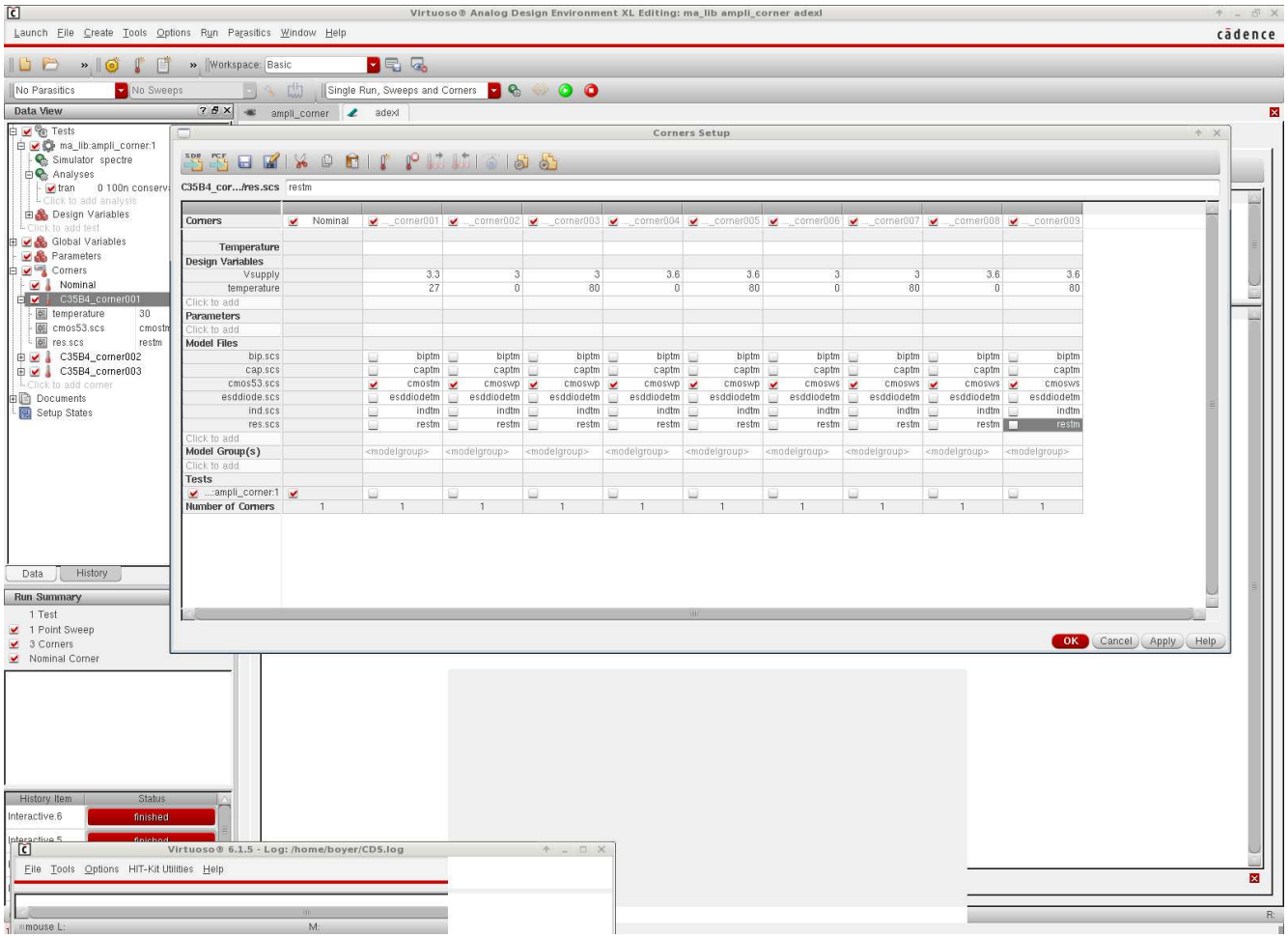

Figure 39 – Selection of corners

In the menu Dataview, ensure that only the corners that you have selected are checked.

Design tips: Power supply voltage corner

The corner on the power supply voltage is called Vsupply. A global variable Vsupply has to be declared. Give the value Vsupply to the power supply voltage generator of your circuit in your schematic diagram.

Launch the simulation by clicking on the icon  . All the activated tests and corners will be launched sequentially. Once the simulation is achieved, right-click on the name of the test and select Direct Plot. The results of the different corner analysis will be plotted on the same graph.

XII. List of shortcuts for Virtuoso Schematic Editor XL

The following table lists the main shortcuts in the schematic editor.

Key	Command
c	Copy
f	Fit window
i	Add instance
l	Label wire
m	Move
p	Add pin
q	Edit parameters
r	Rotate
R + F3	Select sideways to mirror
u	Undo
w	Add wire
z	Zoom to box using left mouse clicks
← →	Move around window
F3	Command options
Left click	Select/click
middle-mouse over objects	Typical properties
right mouse	Repeat last operation
Alt Gr +]	Zoom in
Alt Gr + [	Zoom out
E	Descend (into hierarchy) + read
Shift + E	Descend (into hierarchy) + edit
Ctrl + E	Return to (top) hierarchy

Tableau 1 - Main shortcuts for Virtuoso Schematic Editor

XIII. Local support at AIME

From the website of l'AIME (www.aime-toulouse.fr), you can have a local access to numerous on-line documentations of the software available at AIME. Launch any web navigator to see the link to on-line documentation **(Docs des logiciels**):

- Documentation of Cadence v6.1 and the associated tools and simulators (Virtuoso Schematic Composer, Spectre, Spectre RF, …). Use the link **Cadence**, and **Cadence 6.1 Documentation**.

- Documentation of the design kit AMS Hit Kit v4.10, which contains information about technological process AMS CMOS 0.35 µm, models of transistors, I/Os, ESD protections, etc… The documentation is available from the link **AMS**. Click on **Hit-Kit Online – Documentation 4.10**.