Design of analog CMOS circuits

Design of a fully integrated wireless power transmitter

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I. Glossary

ADC	Analog-to-Digital Converter
BJT	Bipolar Junction Transistor
CAD	Computer-Aided Design
CDM	Charged-Device Model
CMOS	Complementary Metal Oxide Silicon
EDA	Electronic Design Automation
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FOD	Foreign Object Detect
FOD	Foreign Object Detection
HBM	Human Body Model
I/O	Input-Output
IC	Integrated Circuit
LDO	Low Drop-Out (linear voltage regulator)
NTC	Negative Temperature Coefficient
OCP	Over Current Protection
OTP	Over Temperature Protection
PDK	Process Design Kit
PLL	Phase-Locked Loop
POR	Power-on-Reset
PVT	Process-Voltage-Temperature
WPC	Wireless Power Consortium
WPT	Wireless Power Transmitter

II. Intended learning outcomes

The purpose of this course is to acquire the vocabulary, the basic knowledge and expertise, the skills to specify and validate the electronic design of CMOS analog circuits, using a professional CAD environment.

Learning outcomes	**Level**
Know the fundamental building blocks used in analog, RF and digital circuits	Knowledge & comprehension
Understand their operation	Comprehension
Specify the electronic architecture of an integrated circuit from specifications	Application
Use CAD tools to develop and check the operation of CMOS IC project	Application
Analyze the influence of environmental and process effects on IC performance	Analysis
Propose and evaluate IC design solutions to respond to performance criteria	Synthesis & Evaluation

More specifically, the learning outcomes about CMOS analog circuit design are:

1. Create a typical full custom design flow for an analog circuit with an industrial CAD tool, as shown in Figure 1

2. Propose a detailed specification of an electronic circuit, including a functional block-diagram, a list of I/O pins, the power supply and clock domains, an electrical architecture

3. Design a circuit from a process design kit (PDK) (select the available elementary components according to their performances and limits)

4. Perform and analyze the main simulations proposed by professional CAD tools for analog circuit design

5. Optimize the electrical schematic diagram of a circuit and its parameters according to performance, robustness, environmental requirements, and process variation

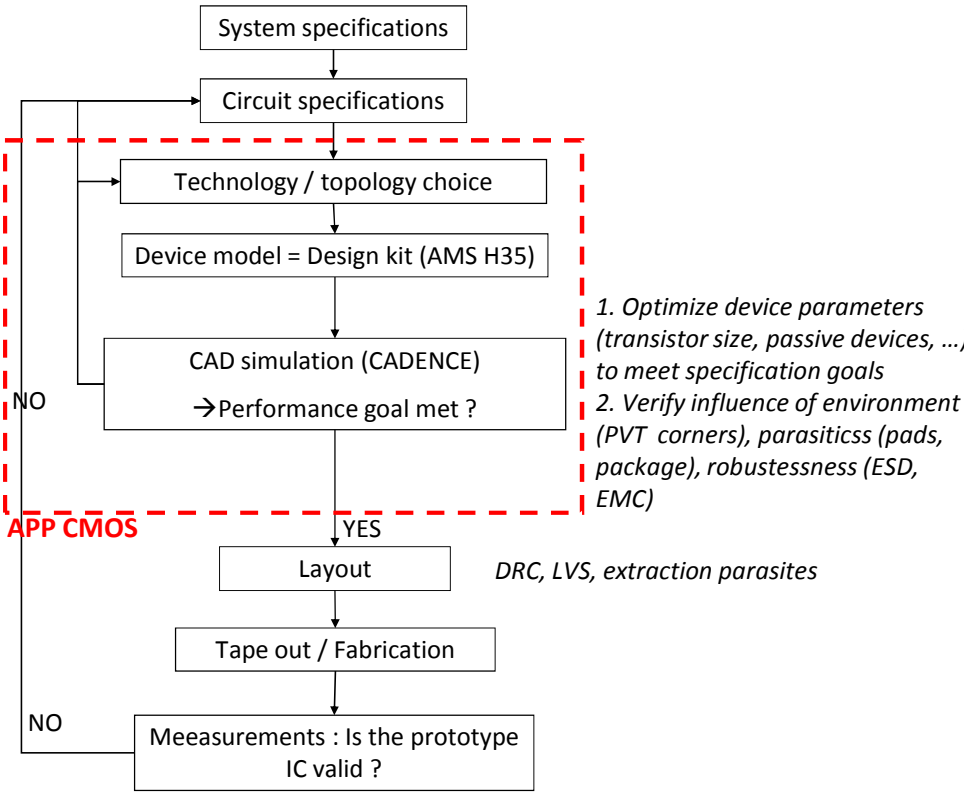


Figure 1 - Typical design flow of analog integrated circuits (full custom design)

III. Planning

The main steps of the project are:

1. Design an architecture of the circuit (block diagram) with all the physical input-outputs
2. Respect all the constraints (functional performances, electrical, environmental, technological constraints, etc.)
3. Propose electrical diagram of some analog/RF blocks of the circuits with associated constraints
4. Write a specifications report containing the previous information
5. Validation and improvement of electrical schematic based on CAD tool (Cadence)
6. Prediction of circuit performances in the different PVT conditions
7. Write a design report (« scientific paper » format) which presents the designed circuit and simulated performances

Figure 2 presents the flowchart of the project planning. There are three types of sessions:

- group work: each group works on the specification of the circuit or on the writing of the reports
- Feedback from the teacher: the teacher provides course materials / feedback to the class

- Lab: each group works on the design of the circuit with the CAD tool at AIME

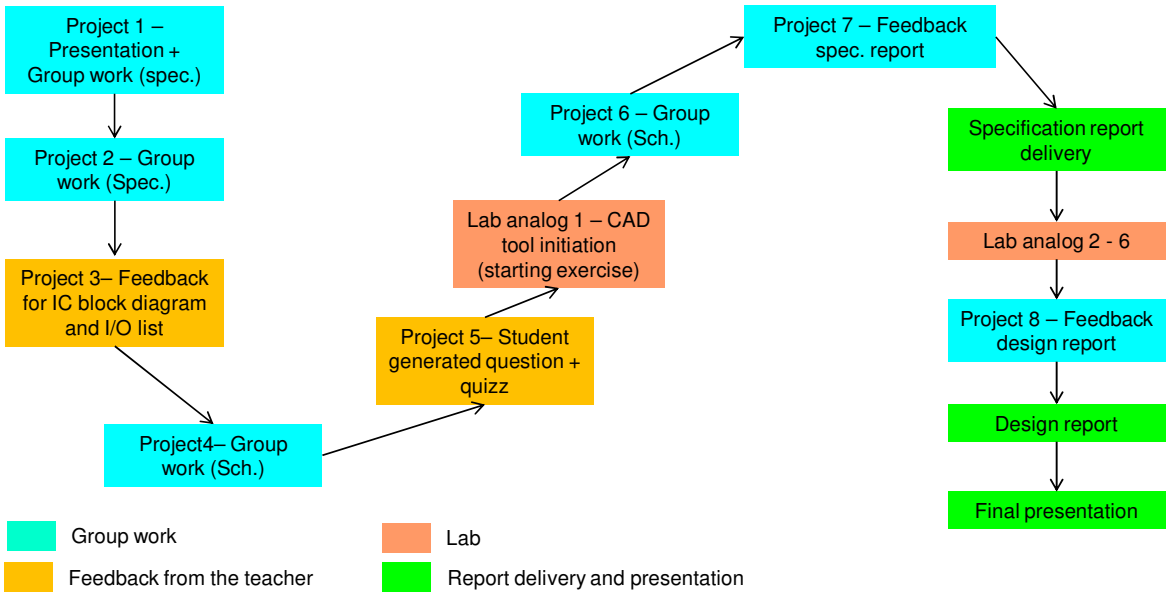


Figure 2 - Flowchart of project planning

The detailed planning is described in the table below. The project is divided in two parts:

- the specification of the circuit
- the design of some analog blocks of the circuit

Week	Activity	Objectives and constraints
40	Project 1	Project presentation Start specifications work
	Project 2	Specifications work (IC block diagram and I/O pin list) IC block diagram and I/O pin list sent **before Wednesday 4/10/2017 23h59**
	Project 3	Feedback on IC block diagram and I/O pin list
41	Project 4	Specifications work (analog blocks and detailed constraints)
	Project 5	Student generated questions and quiz
42	Lab 1	CAD tool initiation
	Project 6	Specifications work (analog blocks and detailed constraints)
43	Lab 2	Functional simulation
44	Project 7	Feedback on initial version of the specifications report
45	Labs 3	Functional simulation
	English validation	Validation of the English of the specifications report by English teacher

	Specification report delivery	Due before **Friday 10/11/2017 at 23h59**
46	Lab 4	Functional simulation
47 - 48	Labs 5 & 6	Performance optimization, PVT corner simulation
49	Project 8	Feedback on initial version of the design report
2	Design report delivery	Due before **Tuesday 09/01/2018 at 23h59**
3	Final presentations (during English course)	**Wednesday 17/01/2018 afternoon**

Important dates:

- Specifications report due date: **Friday 10/11/2017 at 23h59**
- Design report due date: **Tuesday 09/01/2018 at 23h59**
- Final presentations: **Wednesday 17/01/2018**

The reports and the presentation slides must be sent to the following e-mail address: alexandre.boyer@insa-toulouse.fr.

IV. Project assessments

This course is coupled with the English course. The different reports and presentations will be used for the evaluation of English. The mark of the project will be evaluated according to:

- **50 % for the specification reports**
- **50 % for the design reports**

V. Teams

Group 1	Group 2	Group 3

VI. Customer specifications

1. Objective of the project

This project aims at designing a fully integrated wireless power transmitter (WPT) used for a charging station for small electronic mobile devices (e.g. smartphone) in a vehicular environment. It consists of an integrated circuit (IC) which includes all the functional blocks of this transmitter, except the coils and too? two large passive devices. The purpose of integration is the reduction of the number of devices and hence the cost. Figure 3 presents an example of a charging station, where we see mainly the coils. The electronic control is implemented on the other side of the board. Figure 4 summarizes the operating principle of a typical wireless power transfer system. In this document, the receiver is the power receiving circuit and the load to recharge.

The charging station must meet the requirements of the QI standards (version WPC 1.1.2), developed by the Wireless Power Consortium in order to ensure interoperability between all mobile electronic devices. The circuit is supplied directly by the 12 V vehicle battery. It can operate with or without a host external microcontroller. The charging station must deliver a maximum power of 5 W with maximum efficiency of 70 % at least (under optimal conditions).

The circuit will be designed with the High Voltage 50 V CMOS 0.35 µm (H35B4S1) process from Austria MikroSystem (AMS). The CAD tool suite CADENCE will be used for the validation and optimization of the electrical diagrams of the internal blocks that are designed.

Figure 3 - Example of wireless power transmitter (Freescale WCT1001A)

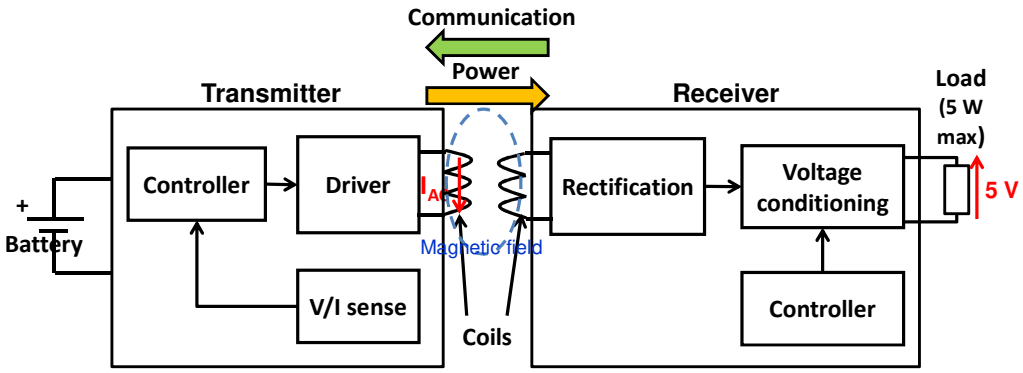


Figure 4 - Principle of a wireless power transmission according to QI standards

2. Circuit functionalities

The transmitter circuit must include the the following functionalities. They are detailed in part 4:

- The overall operation of the circuit is managed by an on-chip digital controller
- The circuit is reset either by an external event through its pin Reset , a Power-On-Reset (POR), or by the appropriate command sent by the host microcontroller through the I2C interface
- The circuit embeds an output buffer which produces the excitation current for the coils (A6 type)
- An on-chip ASK demodulator ensures the reception of radio frames sent by the Qi compliant receiver
- Except for the output buffer, all the internal blocks are supplied by voltages delivered by three on-chip voltage regulators
- The communication with the host microcontroller is based on an I2C interface
- The circuit includes protection against overcurrent (OCP)
- The circuit includes protection against internal overtemperature (OTP)
- The circuit includes protection against excessive heating from nearby environment (NTC)
- The circuit must detect foreign objects placed in the nearby environment (FOD)
- In case of a problem, the circuit sends a fault status to the host microcontroller
- The status of the circuit is indicated by two LED

3. Operating modes

Figure 5 presents a state diagram between the different operating modes of the circuit. They comply with the specification QI WPC 1.1.2.

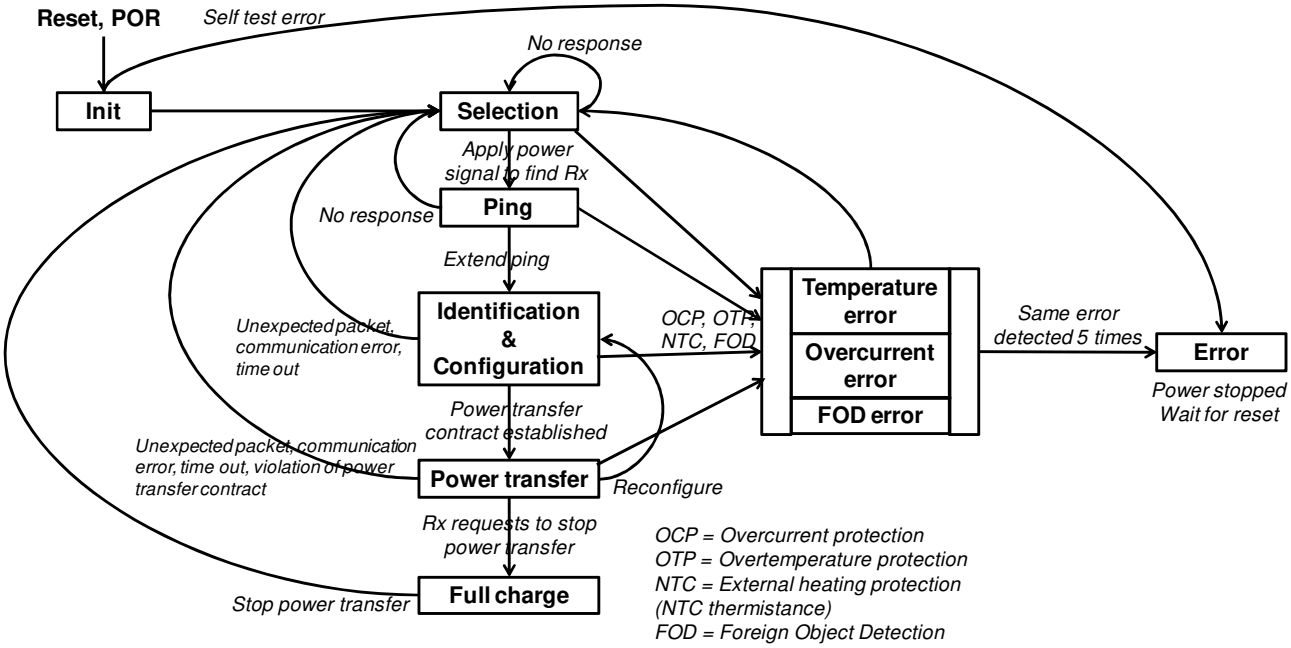


Figure 5 - Operating modes of the WPT circuit

The nominal operating modes are:

- Init Mode: the circuit enters this mode after a POR event, a 0 state applied to its pin Reset, or by the appropriate command sent by the host microcontroller through I2C. The output buffer is left floating. The circuit tests the integrity of internal functions (Self test). The tests are not detailed in this document. If a problem is encountered, the circuit enters Error mode.

- Selection Mode: the transmitter sends short power pings periodically in order to detect a receptor near the charging station. The transmission frequency is set to 175 kHz. In case of a positive answer, it enters Ping mode. Otherwise, it remains in Selection mode. In case of a problem, it enters one of the four Error modes (OCP, OTP, NTC, FOD).

- Ping Mode: the transmitter sends a digital Ping and waits for the answer from the receiver. If it receives a correct answer, it enters Identification & Configuration mode. Otherwise, it returns to Selection mode. In case of a problem, it enters one of the four error modes (OCP, OTP, NTC, FOD).

- Identification & Configuration Mode: the transmitter identifies the receiver and collects configuration information about the required power transfer (maximum power delivered by the receiver to its load). The "power contract" is signed. Then, the transmitter enters Power Transfer mode. If the transmitter is not able to deliver the required power, the transmitter returns to Selection mode. In case of a problem, it enters one of the four Error modes (OCP, OTP, NTC, FOD).

- Power Transfer Mode: the transmitter transfers the power to the receiver continuously. The transmitted power is adjusted according to the content of the frames sent by receiver regularly. The status of the power transfer is indicated to the user through external LED. If the "power contract" is

violated or if a communication error from the receiver to transmitter occurs, the power transfer is stopped and the transmitter returns to Selection mode. In case of a problem, it enters n one of the four Error modes (OCP, OTP, NTC, FOD).

- Full Charge Mode: the circuit enters this mode as soon as the receiver sends the End of Charge frame. The transmitter stops the power transmission and remains in this mode for 5 seconds. The end of power transfer is indicated to the user by external LED. Finally, the transmitter returns to Selection mode.

There are four error modes:

- Temperature Error Mode: the transmitter enters this mode when one of the following two conditions are encountered: excessive internal or external temperature, OTP and NTC errors respectively. The power transfer is stopped and the output buffer is put in high impedance state. The fault status pin is pulled down to '0'. One flag in the error register of the controller is raised (this flag is accessible only through the appropriate I2C command). The error status is indicated to the user by external LED. The transmitter exits this mode when the internal or external temperature goes below a predefined threshold (refer to part 4 for the definition of temperature thresholds) and returns to Selection mode.

- Current Error Mode: the transmitter enters this mode when the current delivered by the output buffer exceeds a predefined limit (refer to part 4 for the definition of current limits). The power transfer is stopped and the output buffer is put in a high impedance state. The fault status pin is pulled down to '0'. One flag in the error register of the controller is raised (this flag is accessible only through the appropriate I2C command). The error status is indicated to the user by external LED. The transmitter remains in this mode for 30 seconds before returning to Selection mode.

- FOD Error Mode: the transmitter enters this mode when a foreign object (conductor) is detected near the charging station. The power transfer is stopped and the output buffer is put in a high impedance state. The fault status pin is pulled down to '0'. One flag in the error register of the controller is raised (this flag is accessible only through the appropriate I2C command). The error status is indicated to the user by external LED. The transmitter remains in this mode for 30 seconds before returning to Selection mode.

- Error Mode: the transmitter enters this mode if the same error condition (OCP, OTP, NTC, FOD) is repeated more than 5 times consecutively or if the Self Test fails. The output buffer is put in a high impedance state. The on-chip voltage regulator which provides the power supply to analog blocks is stopped and the controller enters a safe mode (Error mode). The content of its internal registers is still accessible through I2C commands. It returns to Selection mode only after a Reset.

4. Detailed component specifications

The following parts detail the specifications of the power transmitter circuit. For conciseness, specifications of some blocks are not given.

a. Power supply

The transmitter operates from one energy source: the vehicle battery whose voltage is written V_{BAT}. Its nominal value is 12 V, but the transmitter must operate satisfactorily without any loss of performance with a battery voltage ranging from 7 to 19 V. The battery voltage supplies the output buffer and the on-chip voltage regulator.

The transmitter includes three LDO (Low Drop Out) voltage regulators used for the supply of low voltage blocks:

- LDO_D: this regulator provides the power supply voltage to digital blocks and I/O of the transmitter. It delivers a nominal voltage of 3.3 V +/- 100 mV with a maximum current of 100 mA.
- LDO_A: this regulator provides the power supply voltage to analog blocks of the transmitter. It delivers a nominal voltage of 3.3 V +/- 100 mV with a maximum current of 20 mA.
- $LDO_{4.1}$: this regulator provides the power supply voltage to bias external LED. It delivers a nominal voltage of 4.1 V +/- 100 mV with a maximum current of 30 mA.

An external pin is dedicated to the output of each regulator for decoupling purposes. The number of power supply-ground pairs and the package must be chosen to ensure a proper operation of the circuit and sufficient thermal dissipation.

b. Reset

The transmitter offers three Reset mechanisms:

- Power-On-Reset (POR): when the power supply voltage of the digital controller drops below 2.6 V, the operation of the transmitter stops. Then, when the voltage exceeds 2.8 V, a POR condition is detected.
- Reset pin pulled down to '0': the /Reset pin is used to externally reset the transmitter. If a '0' level is applied on this pin for more than 10 µs, the circuit is forced to enter Reset mode. The transmitter returns to Init mode when level '0' is released (applied voltage greater than 2.4 V). An external pull-up resistor will be placed on this pin.
- Reset I2C command: the host microcontroller may force entry into Reset mode by sending a Reset command through the I2C bus.

In Reset mode, the output buffer is left floating, the internal registers of the controller and I2C interface are reinitialized, PLL and ADC are disabled.

c. Controller

The controller is the central part of the transmitter. It manages the operation of the circuit, mode entry, the command of the output buffer and the power transmitted to the receiver, the processing of the messages received by the demodulator and I2C interface, hardware and software protection and diagnosis of the circuit.

Only the command of the buffer is described in this part. The controller is synchronized by an internal 2 MHz crystal oscillator. The switching frequency of the output buffer varies from 120 and 205 kHz. The duty cycle changes from 10 to 50 %. In selection mode, the frequency is set to 175 kHz and the duty cycle to 50 %. The buffer command signals are synthesized by an internal PLL.

TCommunication with the host microcontroller is made through a serial I2C interface. The host microcontroller can diagnose the state of the transmitter by reading the status and test registers, and force a reset. The I2C bus runs at 100 kHz.

d. Output buffer

The output buffer is compatible with an A6 type coil (refer to QI WPC 1.1.2 specifications). It is loaded by an equivalent LC network, as defined in QI WPC 1.1.2 specifications. The amount of transmitted power is controlled by the frequency and the duty cycle of the buffer command sent by the controller. The controller also sets the dead time of the signal delivered by the output buffer. Each output buffer may deliver a maximum current of 1.5 A. Output buffers are supplied by the car battery directly. They **must** operate over all the voltage range of the battery (see part a). Simulations results **must** prove that the required power (5 W) can be delivered to the load with an efficiency of 70 % at least (under optimal conditions).

e. Demodulation

The demodulation is done by reading the output buffer current. The wireless communication signal is ASK-modulated. The received frames are then transmitted to the controller. The functionalities and the specifications of the demodulator are not detailed here.

f. Analog-to-digital converter

The transmitter contains a 12-bit analog-to-digital converter (ADC). It is used for OTP and FOD safety mechanisms. The conversion result is transferred to the internal register of the controller. The specifications of ADC are not detailed here. The ADC regularly captures the output buffer voltage and the power supply voltage (FOD mechanisms) and the internal temperature (SW-OTP mechanism).

g. Overcurrent Protection (OCP)

When the amplitude of the current delivered by the three output buffers exceeds 4.5 A +/- 0.1 A, the OCP protection mechanism is triggered. A measurement of the current is made by the circuit. The proposed circuit must be able to measure **both** positive and negative currents. An internal analog block will detect excessive current and set the OTP signal to '1'. This signal is sent to the controller. The transmitter enters Current Error mode. The This error **must** be triggered in less than 100 µs. The gain and the bandwidth of the current acquisition chain **must** be specified.

h. Overtemperature Protection (OTP)

The transmitter includes two overtemperature protection mechanisms:

- Software OTP (SW-OTP): this protection mechanism is triggered when the internal temperature exceeds 120 °c +/- 1°c. It leads to an entry into Temperature Error mode. As soon as the internal temperature goes below 80°c +/- 1°c, the transmitters leaves this mode and returns to Selection mode. SW-OTP is based on an internal temperature sensor and the ADC.

- Hardware OTP (HW-OTP): this redundant safety mechanism triggers if the SW-OTP mechanism fails. It triggers when the internal temperature is comprised between 125°c and 150°c. It leads to an entry into Temperature Error mode. As soon as the internal temperature goes below 80°c +/- 1°c, the transmitters leaves this mode and returns to Selection mode. SW-OTP is based on an internal temperature sensor which delivers the digital signal HW-OTP to the controller. This signal is set to '1' when the internal temperature becomes excessive.

The gain and the bandwidth of the OTP acquisition chain **must** be specified.

i. External overheating Protection (NTC)

The transmitter includes a protection mechanism against excessive heating in the surrounding environment. It is based on an external Negative Temperature Coefficient (NTC) resistor. The NTC network is biased?? by the power supply V_{DDA} and is connected to the pin Tsense. The protection mechanism is triggered when the external temperature exceeds 65°c +/- 2°c and leads to an entry into Temperature Error mode. As soon as the external temperature drops below 60°c +/- 2°c, the transmitter returns to Selection mode. The NTC mechanism is triggered by an analog block when the voltage applied to the Tsense pin is less than 1 V. An internal signal NTC is set to '1' and transmitted to the controller. The characteristics of the external NTC resistor and its biasing **must** be specified.

j. Foreign Object Detection (FOD)

A detection mechanism of foreign objects is included to prevent the heating of nearby metallic objects during power transfer. This mechanism is based on the comparison between the power which is transmitted and received. The receiver sends frames regularly to adjust the amount of power transmitted. The power transmitted is estimated by a measurement of the output buffer power supply and the current delivered by the three output buffers.

If the power received is less than the power transmitted minus a margin called the Threshold, the FOD mechanism is triggered. The transmitter enters FOD Error mode. The accuracy of the voltage reading must be less than 5 mV. The accuracy of the current reading must be less than 3 mA. By default, the Threshold is set to 250 mW. It can be adjusted (+100 mW, +200 mW, -100 mW) using two digital input pins.

k. Fault status pin

An output pin called /FS (Fault Status) is set to '0' when the transmitter enters an error mode. This state is released when the transmitter returns to a nominal mode. An external pull-up resistor is placed on the pin /FS.

l. LED driver

Two external LEDs called LED1 et LED2 indicate the operating state of the transmitter according to the table below.

MODE	Selection, Ping, Identification & Config.	Power transfer	Full charge	Error (OTP, NTC, OCP)	FOD Error

LED1	OFF	ON	Blink 0.5s	OFF	OFF
LED2	OFF	OFF	OFF	ON	Blink 0.5 s

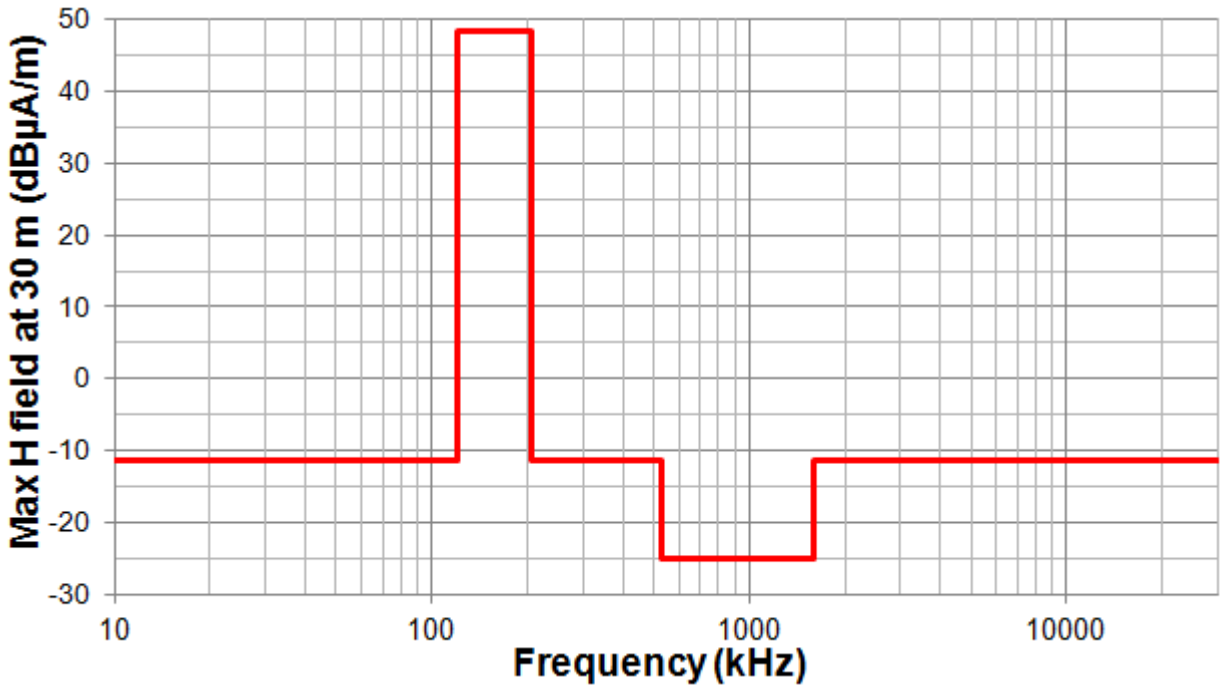
5. Expected electrical characteristics

	Parameters	**Values**
Power supply voltage	Battery voltage V_{BAT}	7 - 19 V
Output voltage	Maximum current	4.5 A
	Switching frequency	120 - 205 kHz
	Duty cycle	10 - 50 %
	High-side output voltage	> VBAT - 4.7 V
	Low-side output voltage	< 3.8 V
LDO - Digital blocks	Output voltage V_{DDD}	3.2 - 3.4 V
	Maximum current	50 mA
LDO - Analog blocks	Output voltage V_{DDA}	3.2 - 3.4 V
	Maximum current	15 mA
LDO - LED	Output voltage $V_{DD4.1}$	4 - 4.2 V
	Maximum current	30 mA
Digital I/O	V_{OL}, I_{OL}	0.3 V, 6 mA
	V_{OH}, I_{OH}	V_{DDD}-0.6 V, 6 mA
	V_{IH}	2.1 V
	V_{IL}	1.4 V

6. Environmental, robustness, EMC constraints

	Parameters	**Values**
Temperature range	Storage temperature	-40°c - +150°C
	Operating ambient temperature	-40°c - +80°c
	Operating junction temperature	-40°c - +125°C
ESD	HBM	+/- 2 kV
	CDM	+/- 750 V

The power transmitter circuit will be mounted in applications which **must** comply with the EMC standard EN55011 (for industrial, scientific, medical devices). This standard defines limits for conducted and radiated electromagnetic emissions. The graph below shows the limits of the magnetic field at 30 meters.



The transmitter must be qualified AEC-Q100 revision G - Grade 3.

7. Analog blocks to design

In this project, you will design and validate the schematic diagram for the following analog blocks:

- the output buffer and its command
- the internal temperature sensor and the triggering of HW-OTP
- the measurement chain of the current delivered by the output buffer and the triggering of OCP
- the triggering of NTC

8. Simulation hypothesis

Simulations of all the internal devices may be based on the Hit Kit AMS H35 process design kit (PDK).

The transmitting coil is modeled with? a 12.5 µH inductance. Its resonant frequency and its quality are are14 MHz and 100 at 125 kHz respectively. The receiving coil is modeled with/on a 11 µH inductance. Its resonant frequency and its quality are 16 MHz and 30 at 125 kHz respectively.

The magnetic coupling factor between transmitting and receiving coil depends on the distance and varies between 0.3 and 0.6.

The model of the rectifier and the load on the receiver side is simplified to a constant resistor of 5 Ω to ensure a transmitted active power of 5 W under 5 V. The switching block of the receiver is not taken into account.

By default, all the modeled analog blocks will be loaded by a 0.1 pF capacitance, except if a more precise value is determined.

VII. Deliveralbes

During this project, you are required to:

- **1. Write a detailed specifications reports of the circuit. This document must be written in English using the proposed template.**
- **2. Propose and optimize an electrical schematic diagram of the analog blocks under CADENCE.**
- **3. Write a report which explains the principle and the improvements of the proposed design, summarizes the expected performances (justified by simulation results). This document must be written in English using the proposed template.**
- **4. Present the work of your team during the final presentation (English course).**

Deadlines for the reports:

- Specifications report: **Friday 10/11/2017 at 23h59**
- Design report: **Tuesday 09/01/2018 at 23h59**
- Final presentations: **Wednesday 17/01/2018**

The reports and the presentation slides must be sent to the following e-mail address: alexandre.boyer@insa-toulouse.fr.

1. Template for the specifications report

The template of the specifications report is found on the website www.alexandre-boyer.fr/enseignements in the following document: Specification_report_WPT_GpeX_2016.doc.

The specification report must include:

- a brief explanation of the operating principles of the circuit
- a block diagram of the circuit, showing the main internal blocks, the power supply domains, the clock, the analog/digital signals between the blocks
- a list of the input-output pins of the circuit, their nature and the associated constraints
- a summary of the specifications that the circuit must fulfill
- the detailed specifications of the analog blocks that will be designed

Use concise and clear sentences, use appropriate vocabulary, use schematic diagrams, tables and graphs. Ensure that all the units and legends provided are correct. Ensure that the figures are clear and readable.

2. Template for the design report

The template of the design report is found on the website www.alexandre-boyer.fr/enseignements by the following document: Fiche synthese English version.doc.

The design report follows the typical template of a scientific article. It should not exceed 8 pages with annexes. This report must include:

- a brief reminder of the designed circuit and the main performances expected
- the detailed electrical schematic diagram of the designed analog blocks
- an explanation of the operating principle of the designed analog blocks, and the main adjustments made to optimize performances
- a summary of the simulated performances
- the simulation results that demonstrate compliance with the required functional performances, or the validity of the optimization process
- the simulation results that demonstrate compliance with the required environmental performances, or the validity of the optimization process
- the analysis of the performances obtained
- the perspectives to improve circuit performances or simulations

Use concise and clear sentences, use appropriate vocabulary, use schematic diagrams, tables and graphs. Ensure that all the units and legends provided are correct. Ensure that the figures are clear and readable.

VIII. Support

The following documents can be downloaded from www.alexandre-boyer.fr/enseignements or are available at the INSA library:

Basic notions about CMOS analog design	Course 4AE "Etude et modélisation des composants actifs" E. Sicard, S. Ben Dhia, "Basic CMOS Cell Design", Mc Graw Hill, 2006 Gray, Hurst, Lewis, Meyer, "Analysis and Design of Analog Integrated Circuits - 5th Edition" (chapters 4, 6, 7 and 9) On-line MOOC: ▪ https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-012-microelectronic-devices-and-circuits-fall-2009/ ▪ https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-012-microelectronic-devices-and-circuits-spring-2009/lecture-notes/
QI Specifications	"System Description Wireless Power Transfer - Vol 1: Low Power - Part 1: Interface Definition - version 1.1.2", June 2013
AMS CMOS 0.35 µm process and PDK information (available at AIME	▪ ENG-238, "0.35 µm 50 V CMOS Process Parameters - revision 6.0", Austria MikoSystems, 2009 ▪ ENG-298, "0.35 µm 50 V CMOS Parasitic Devices - revision 3.0", Austria MikoSystems, 2014
Student reports of	▪ CMOS design report - Aniba Benkhalfia de Reviers Saint-Martin.pdf: design

previous years	report 2014-2015 (former project - 1.23 V bandgap voltage reference) ▪ Design_Report_CMOS_Grp2_2015-01-8.docx : design report Gpe 2 2015-2016 ▪ Design_report CMOS group3.pdf : design report Gpe 3 2015-2016 ▪ EBLVB1_article_Grp1.pdf : design report Gpe 1 2016-2017 ▪ FINAL_PRESENTATION_EBLVB1.pdf: final presentation Gpe 1 2016-17 ▪ Rapport_conception_CMOS_Bosbin_Chatelais_Harras_Roques_Grp2.pdf: design report Gpe 2 2016-2017 ▪ Design presentation_Gpe2.pdf: final presentation Gpe 2 2016-2017 ▪ CMOS_Design_Report_Grp3.pdf: design report Gpe 3 2016-17 ▪ CMOS_Presentation_Grp3.pdf: final presentation Gpe 3 2016-2017